GERMAN - MONGOLIAN INSTITUTE FOR RESOURCES AND TECHNOLOGY

The present work was submitted to

the German-Mongolian Institute of Resources and Technology

Revised Scope: Design and Implementation of a Portable Bus-Powered Dual-Mono USB-C DAC/AMP on the XMOS XU208 Platform

Bachelor's Thesis

By

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Statutory Declaration

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I hereby affirm in lieu of an oath that I provided the submitted bachelor thesis

Revised Scope: Design and Implementation of a Portable Bus-Powered Dual-Mono USB-C DAC/AMP on the XMOS XU208 Platform

I did not use any sources other than those stated. In case that the work is additionally submitted on a data medium, I declare that the written and the electronic form are completely identical. The work was not submitted in the same or similar form to any examination authority.

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1. Introduction

AI tools (e.g., ChatGPT/Claude/Gemini) were used for language refinement, structural formatting, and LaTeX equation rendering; however, all engineering decisions, simulations, and circuit architectures are the original work of the author.

1.1 Background

This thesis documents the complete hardware engineering design cycle of a portable USB-C Digital-to-Analog Converter and headphone amplifier (DAC/AMP), from initial concept through two distinct architectures and three design revisions to a fabricated 4-layer mixed-signal PCB ready for assembly and verification.

The project originated as a desktop DAC/AMP featuring a vacuum tube amplifier stage, solid-state op-amp stage, and an ESS9039Q2M DAC driven by an ESP32-C3 microcontroller. Extensive LTSPICE simulation of the power supply unit — including a MOSFET-based capacitance multiplier achieving a calculated power rail SNR of −112.12 dB — demonstrated the technical viability of the analog design, but the combined financial burden of the triple-transformer architecture, premium components, CNC-milled aluminum enclosure, and the fundamental electromagnetic incompatibility of integrating a WiFi/Bluetooth-enabled MCU into a mixed-signal circuit rendered the desktop architecture undeliverable within the project timeframe and budget.

The subsequent pivot to a portable bus-powered architecture preserved the core design objectives — low-noise power delivery, high interchannel isolation, and jitter-free clock distribution — while reframing them within the constraints of a USB 2.0 500 mA power envelope and a compact dongle form factor. The final design employs the XMOS XU208 USB audio processor, a true dual-mono topology using two independent Cirrus Logic CS43131-CNZR DAC/AMP chips, three independent crystal oscillators, a multi-stage cascaded power distribution network, and both 3.5 mm single-ended and 4.4 mm balanced outputs — an architectural combination not currently found in any commercially available bus-powered portable device.

1.2 Motivation

The motivation for this thesis lies at the intersection of personal domain expertise and academic engineering training. As an audiophile and in-ear monitor collector, signal integrity in high-fidelity audio reproduction is a subject of direct personal interest: the audible consequences of power supply noise, clock jitter, and interchannel crosstalk are not abstract specifications but perceptible differences in listening quality. This pre-existing domain knowledge informed the component selection, architectural decisions, and performance targets throughout the design process.

The technical foundation was established through the Electronics (EEEM304) and Power Electronics (EEEM307) modules, which provided the analytical tools for power supply design, noise analysis, and circuit simulation applied extensively in this thesis. The project extends these foundations into mixed-signal PCB design, electromagnetic compatibility, and USB audio protocol compliance — areas not covered in the standard curriculum but essential to the design problem addressed.

At the core of this work is the challenge central to all high-resolution audio hardware and, more broadly, to mixed-signal electronics design: managing the electromagnetic environment in which sensitive analog circuits coexist with high-speed digital subsystems. This encompasses unbroken ground plane design, differential pair routing for USB 2.0 compliance, controlled-impedance trace geometry, isolated power supply domains, noise-aware component selection and placement, and impedance-matched high-speed signal distribution. The thesis documents how these principles were applied across each design revision, with each iteration refining the electromagnetic architecture in response to specific technical constraints identified in the preceding version.

Component selection, circuit architecture, PCB stackup design, and electromagnetic compatibility decisions were derived from manufacturer hardware design guides, component datasheets, established EMC literature, and the open-source XMOS development ecosystem rather than from supervised instruction in the specific application domain.

2. Market Analysis and Technical Review

The portable USB Digital-to-Analog Converter and headphone amplifier (DAC/AMP) dongle market has expanded rapidly in response to the removal of the 3.5mm headphone jack from mainstream smartphones and the parallel growth of the in-ear monitor (IEM) community. The result is a fragmented market spanning a wide price range — from sub-$20 budget dongles to $300+ audiophile-grade devices — with significant variation in engineering quality, component selection, and output performance. This section surveys the current state of the market across price segments and identifies the technical limitations that motivated the design approach taken in this thesis.

2.1 Budget Segment: Jade Audio JA11

The budget segment, typically priced below $30, is dominated by devices built around low-cost proprietary DAC/AMP system-on-chip solutions. The JCally JM6 Pro [1] and Jade Audio JA11 [2] are representative examples. The Jade Audio JA11 integrates the DAC conversion and headphone amplification into a single proprietary SoC, while the JCally JM6 Pro uses a low-cost dual-chip solution pairing the Conexant CX31993 DAC with a MAX97220 amplifier, achieving 60mW@32Ω — competitive at its price point but still constrained by budget PDN architecture and the absence of balanced output. Both approaches minimize bill-of-materials cost but impose significant performance constraints. Single-chip/low-power dual chip solutions of this class typically offer limited output voltage swing, inadequate current delivery for low-impedance planar magnetic headphones and high-sensitivity IEMs, and restricted SNR performance due to the proximity of digital switching noise to the analog output stage within the same or closely integrated silicon. The Jade Audio JA11 in particular exhibits insufficient output power for demanding loads — a limitation directly attributable to the output stage architecture of its integrated chip rather than any external circuit deficiency. Neither device offers a balanced output, restricting users to single-ended 3.5mm connections and foregoing the common-mode noise rejection and additional voltage swing that a balanced topology provides. The power distribution networks of budget dongles are typically single-stage, drawing directly from USB VBUS through minimal filtering, which exposes the DAC's analog supply to the switching noise present on the USB power bus of a smartphone or laptop.

2.2 Mid-Range Segment: FiiO KA11

The FiiO KA11 [3] occupies the mid-range segment at approximately $30-40 and represents a meaningful step up in output performance and build quality. The KA11 offers a 3.5mm single-ended connection, with the options of having a USB-C input or a Lightning input. However, the physical implementation of the CS43131 DAC chip in a dongle form results in a connector housing that is notably bulky relative to the board dimensions. From an engineering standpoint, mid-range devices in this class typically employ a single stereo DAC chip driving both output stages, meaning the interchannel isolation is limited to the per-chip specification rather than benefiting from complete physical channel separation. Clock architecture at this price point is generally Phase-Locked Loop (PLL) derived from the USB reference rather than sourced from independent crystal oscillators, introducing accumulated phase noise at the DAC input that limits the theoretical THD+N floor.

2.3 High-End Segment: Moondrop Dawn Pro, iFi GO Bar, and XMOS-based Desktop Devices

The high-end portable DAC/AMP segment is represented by devices such as the Moondrop Dawn Pro [4] and the iFi GO Bar [5], both priced in the $50-300 range. These devices demonstrate what is achievable with careful component selection and more sophisticated circuit architecture — the Dawn Pro in particular delivers competitive measured performance at its price point. However, the primary constraint at this segment is cost: the premium performance of devices like the iFi GO Bar is reflected directly in their retail price, placing them out of reach for a significant portion of the target market. The engineering approaches that enable their performance — careful power supply design, high-quality DAC chips, balanced output topologies — are not inherently expensive to implement; rather, the retail price premium reflects brand positioning, industrial design, and manufacturing overhead rather than fundamental component cost barriers.

The XMOS XU208 USB audio processor, the MCU at the heart of the design presented in this thesis, is an established platform in the desktop DAC segment. The Topping D10 [6] and Khadas Tone 2 Pro [7] are representative examples of desktop

devices built around the XU208/XU216, where its deterministic xCORE architecture, USB Audio Class 2.0 [18] compliance, and open-source sc_usb_audio firmware stack [26] have made it a preferred choice for bit-perfect high-resolution audio transmission. Both devices leverage the XMOS platform's 32-bit/384kHz PCM capability and driver-free operation on macOS and Linux, demonstrating the chip's proven track record in demanding audio applications. Critically, however, both the Topping D10 and Khadas Tone 2 Pro are desktop devices powered from dedicated power supplies or USB ports on powered hubs — they are not constrained by the power budget of a smartphone USB-C output. The design challenge addressed in this thesis is the adaptation of the XU208 platform to a bus-powered portable dongle form factor, where the entire device must operate within the USB 2.0 500mA current envelope while maintaining the signal integrity and noise performance associated with desktop implementations. This constraint drives the multi-stage cascaded PDN architecture, the low-power CS43131 DAC/AMP selection, and the compact 4-layer mixed-signal PCB layout documented in the following sections.

2.4 Identified Research Gap and Design Motivation

Across all price segments, several recurring technical limitations are identifiable. Budget devices sacrifice output performance and noise floor through single-chip integration and inadequate power distribution. Mid-range devices address output topology but typically retain single-stereo DAC architectures and PLL-derived clock sources that limit achievable THD+N. High-end devices deliver strong measured performance but at price points that reflect market positioning rather than component cost. Existing XMOS XU208 implementations are restricted to the desktop segment, where power budget constraints do not apply.

The design presented in this thesis addresses these limitations through a combination of approaches not typically found simultaneously at any price point in the current market: a true dual-mono architecture using two independent CS43131-CNZR DAC/AMP chips providing complete physical channel separation and greater than 110dB interchannel isolation across the full signal path; three independent crystal oscillators providing jitter-free master clocks to the DAC chips without PLL-derived phase noise accumulation; a multi-stage cascaded power distribution network using the TPS7A9101, LT3045, and SGM2036 regulators in a noise-aware hierarchy that isolates the analog supply chain from USB VBUS noise through two stages of regulation; and

both 3.5mm single-ended and 4.4mm balanced outputs on a compact 4-layer mixed-signal PCB. The result is a design whose architecture is benchmarked against high-end commercial products while remaining manufacturable at a component cost consistent with the mid-range segment, and whose MCU platform — the XMOS XU208 — is brought to the portable bus-powered domain for the first time in this configuration.

3. Materials, Methods and Design

3.1 The Version 1.0

As outlined in the thesis assignment sheet, the main objective for this thesis was the design, implementation, assembly and testing of a high performance ESP32 based Desktop DAC/AMP with dual amplifier topologies: a vacuum tube stage and a solid state op-amp stage. However, the optimistic sentiment had several critical issues: electromagnetic interference (EMI), exacerbated by the WiFi and Bluetooth antennas of the MCU, the ESP32-C3, financial burden placed by the triple-transformer setup of the quad full bridge rectifier architecture of the PSU, cost of the vacuum tubes, state of the art components (ESS9039Q2M DAC, ADAU1467 DSP, LT1964-BYP and LT1763 op-amp chips), and the planned full CNC-milled solid aluminum enclosure.

The subsequent PSU simulations proved the complexity of the op-amp PSU architecture itself: 68.9 turns ratio transformer is impossible to source, and the outputs themselves failed to reach the stable 15V target without extreme heat dissipation, excessive oscillations and ripples by the low-dropout regulators LT1964-BYP, LT1763.

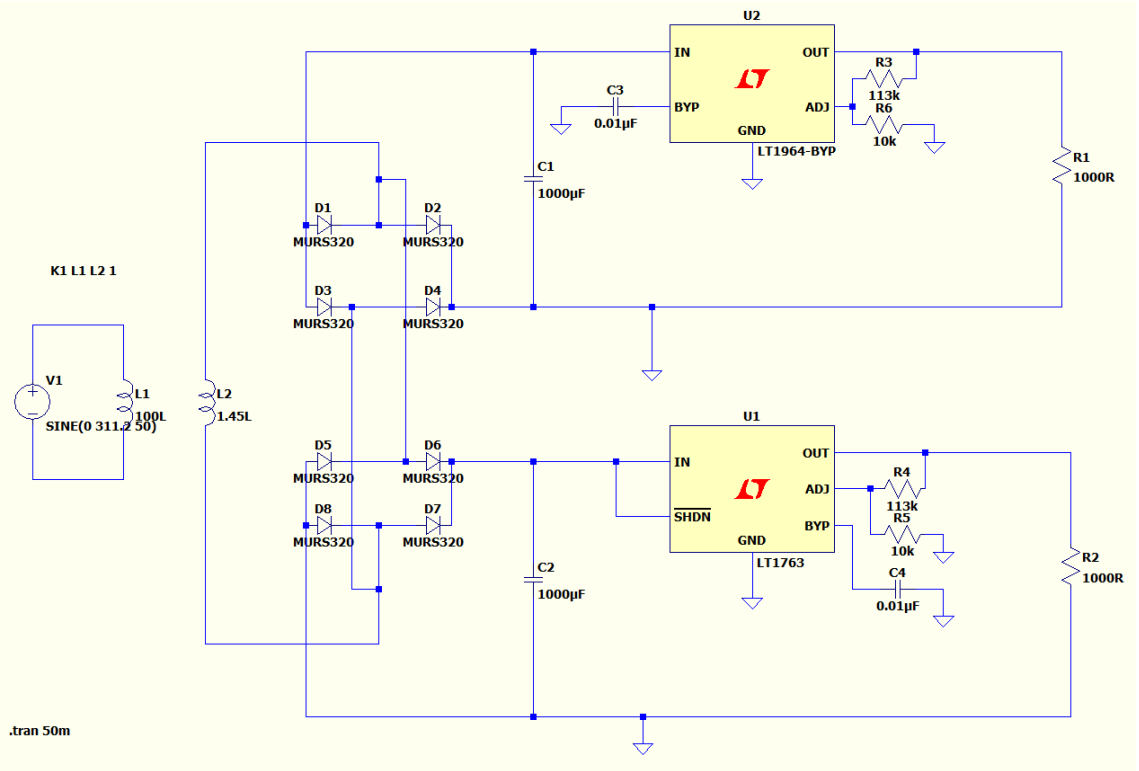


Figure 1: LTSPICE Op-Amp PSU circuit schematic

The op-amp power circuit utilized a single transformer, double full bridge rectifier architecture to achieve the positive-negative power rails needed for the solid-state amplifiers and aimed at reducing the cost.

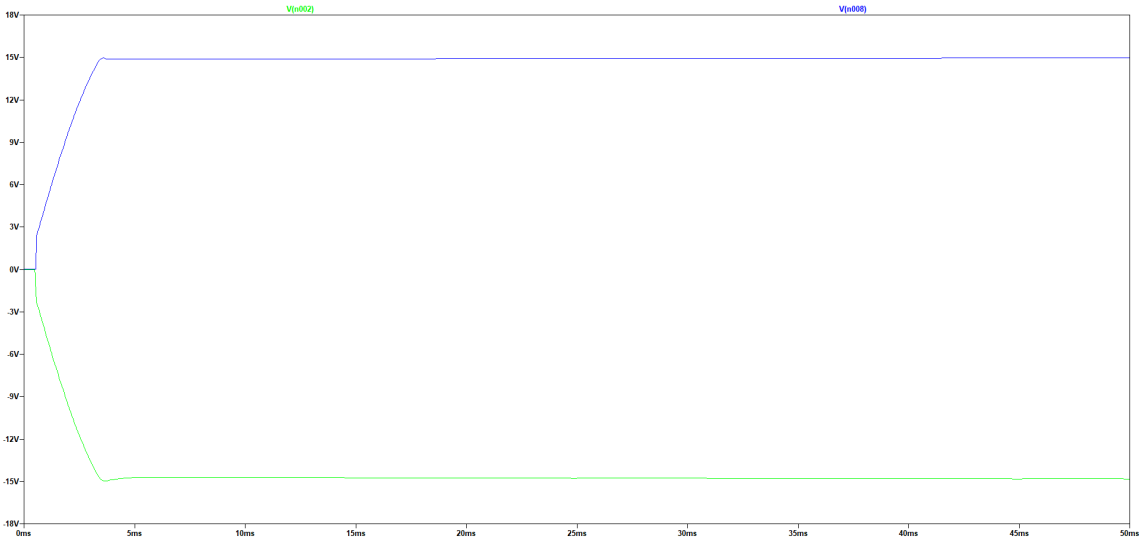


Figure 2: LTSPICE Op-Amp schematic voltage readings (+15V) and (-15V)

The Voltage readings were promising: stable, smooth startup ramp with minimal overshoot or oscillations; stable, flat regulation at 14.78V-15.01V and -14.7V-14.82V once regulated, well within the acceptable operating limits by most op-amp chips.

However, the FFT plot showed a completely different story:

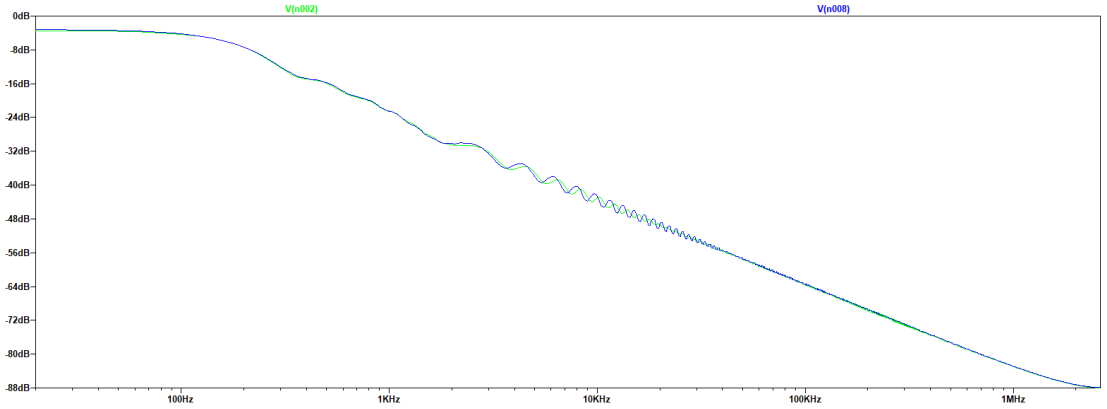


Figure 3: LTSPICE Simulation of the Op-Amp Power Rail showing significant voltage ripple and instability between 1kHz and 100kHz.

As shown in the FFT of the outputs on the Figure 3, the jagged, irregular oscillations, potentially caused by the rectification noise, specifically at the 100Hz-20kHz ranges are audible to the human ear, which is catastrophic for several reasons:

- Audible hiss, hum, or artifacts
- The ripples in the ultrasonic range can fold back through intermodulation distortion (IMD) or aliasing back into audible range, causing further degradation of the signal quality
- Severely limit the noise floor and SNR of the setup.

However, the high voltage rail of the Vacuum tubes (280V) had much more promising results: the implementation of MOSFET-based capacitance multiplier architecture ensured pristine, slow startup voltage across the power rails.

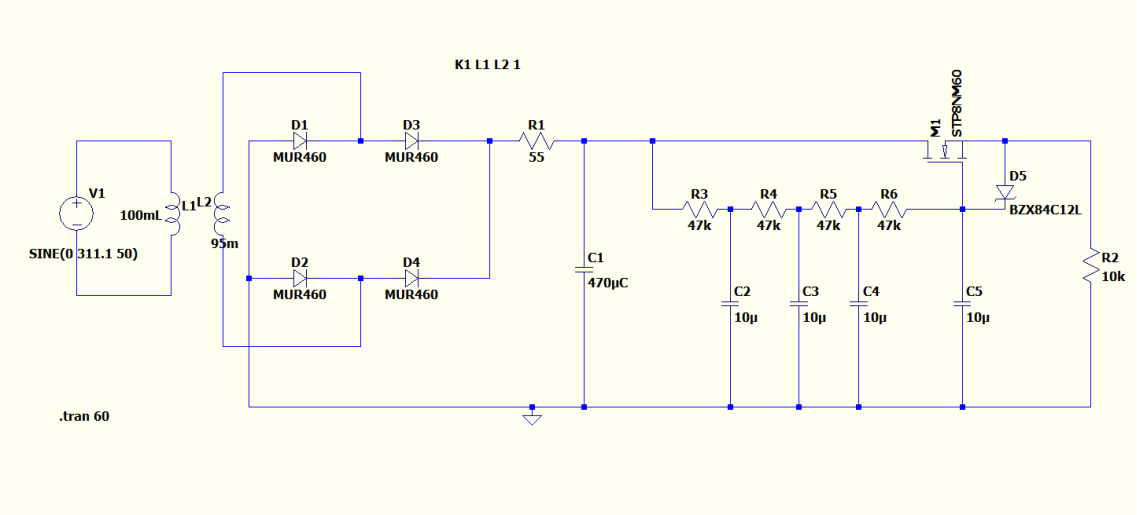


Figure 4: LTSPICE 280V PSU schematic

This architecture given in Figure 4, utilizing a 4-stage RC filter with a MOSFET regulator and a zener protection ensured a 25-second slow startup: a premium feature aimed at extending the life of the vacuum tubes by shielding them from sudden voltage spikes and inrush current with the added benefit of cost and space reduction of the massive capacitors needed for the same filtering output.

3.1.1 Calculations

1. Transformer stage:

   The 311.2V peak mains voltage is derived from the 220V RMS mains supply through the relationship:

$$V_{peak} = V_{rms} \times \sqrt{2} = 220 \times \sqrt{2} = 311.2V \quad (1)$$

$$n = \sqrt{\frac{L1}{L2}} = 0.9747 \quad (2)$$

$$V_{sec(pk)} = 311.2V \times 0.9747 \approx 303.2V \quad (3)$$

   The 303.2V peak secondary voltage provides the raw input to the rectification stage, from which the 280V vacuum tube rail is derived through rectification, passive filtering, and active regulation. The turns ratio of 0.9747 steps this down marginally to 303.2V peak secondary voltage

2. Rectification stage:

   The MUR460 [24] fast recovery diode is retained for the high voltage stage for the same switching noise reasons outlined in the op-amp PSU analysis. In the high voltage context its selection is additionally motivated by its 400V peak inverse voltage rating — essential for reliable operation in a 280V+ DC circuit where voltage transients during switching can significantly exceed the nominal rail voltage.

$$V_{raw} = 303.2V - 2 \times 1.1V \approx 301V \quad (4)$$

3. Passive Filtering stage (R1-C1):

$$I_{load} = \frac{295V}{10000\Omega} = 29.5mA \quad (5)$$

$$V_{drop(C1)} = I \times R = 0.0295A \times 55\Omega \approx 1.6V \quad (6)$$

$$V_{C1} = 301V - 1.6V = 299.4V \quad (7)$$

$$V_{ripple} = \frac{I_{load}}{2f \times C} = \frac{0.0295A}{2 \times 50 \times 0.00047F} = 0.62V_{pp} \quad (8)$$

   The 470µF bulk capacitor C1 provides the primary charge reservoir for the rectified supply. Its large capacitance relative to the load current results in the 0.62Vpp ripple — a relatively low figure that reflects the generous capacitance

budget allocated to this stage. The subsequent RC filter stages reduce this further to the millivolt level before the voltage reaches the vacuum tube anodes.

4. Ripple control:

   The 4-stage RC network following C1 provides cascaded attenuation of the residual ripple. Each stage consists of a 47kΩ series resistor and a 10μF shunt capacitor, giving a cutoff frequency of:

$$f_C = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 47000\Omega \times 0.00001} \approx 0.33Hz \quad (9)$$

$$A = \frac{f_{ripple}}{f_C} = \frac{100Hz}{0.33Hz} = 300 \quad (10)$$

$$V_{ripple(out)} = \frac{V_{ripple}}{A} = \frac{0.62V_{pp}}{300} = 2.07mV \quad (11)$$

   The 0.33Hz cutoff frequency of each RC stage is deliberately set far below the 100Hz ripple frequency, ensuring that the ripple component sees an attenuation of 300 per stage. With four cascaded stages the theoretical attenuation would be 300^4 — however in practice the stages interact through the MOSFET gate impedance and the output impedance of each stage loads the previous one, reducing the effective attenuation. The LTSPICE simulation captures these non-ideal interactions and produces the measured 2.07mV output ripple that the single-stage calculation predicts, confirming that the dominant attenuation is provided by the first RC stage and the MOSFET regulator rather than by the cascaded stages acting independently.

   The slow-start behavior is an emergent property of this RC network: on power-up, the large time constant of each RC stage (τ = 47kΩ × 10μF = 470ms per stage, four stages in series giving an effective startup time of approximately 25 seconds) means the gate voltage rises gradually rather than instantaneously. This protects the vacuum tubes from the inrush current and voltage spike that would occur if the full 280V were applied immediately — a critical feature for extending tube life, as vacuum tubes are particularly vulnerable to cathode damage during cold startup.

5. MOSFET calculation:

   Source pin follows the Gate Voltage minus the threshold Voltage ($V_{GS(th)}$)

   For STP8N60 [23], the threshold voltage is $V_{GS(th)} = 3.0 \sim 5.0V$

$$V_{out} = V_{gate} - V_{GS(th)} = 299.4 - 4.0V = 295,4V \quad (12)$$

$$W_{diss} = V_{GS(drop)} \times I_{load} = 4.0V \times 0.0295A = 0.118W \quad (13)$$

The STP8N60 operates with minimal power dissipation at this load current — 0.118W is well within the device's continuous power rating without heatsinking. The source follower configuration means the MOSFET presents a low output impedance to the load, maintaining regulation against load current variations without the feedback loop complexity of an op-amp based regulator.

6. Ripple, THD+N calculations:

$$V_{noise(rms)} = V_{ripple(out)}/2\sqrt{2} = 0.000207V/2\sqrt{2} = 731.8uV \quad (14)$$

$$SNR = 20 \times log_{10}(\frac{V_{noise}}{V_{DC}}) = 20 \times log_{10}(\frac{0.00007318V}{295.4V}) = -112.12dB \quad (15)$$

The -112.12dB SNR of the 280V rail is well suited to the vacuum tube application. Valve amplifiers operating from high voltage rails are inherently limited in SNR by the tube's own shot noise and thermal noise contributions, which typically produce noise floors in the -80dB to -100dB range. A power supply SNR of -112.12dB therefore presents no meaningful limitation to the amplifier's achievable noise floor — the tube itself will be the dominant noise source, not the power supply.

7. Resistor thermal noise calculation (Johnson-Nyquist noise) [22]:

$$V_{noise} = \sqrt{4K_bTR\Delta f} = \sqrt{4 \times 1.38 \times 10^{-23} \times 300K \times 99.67Hz} = 1.28nV \quad (16)$$

As in the op-amp PSU analysis, the 1.28nV thermal noise floor of the resistive network is negligible relative to the ripple-derived noise and the inherent noise of the vacuum tube stage. The Johnson-Nyquist calculation confirms that the resistor selection in the RC filter network introduces no meaningful noise contribution — the dominant noise sources are the ripple from rectification and the intrinsic device noise of the vacuum tubes themselves.

However, there was 11.9V (3.8%) deviation from the calculated Voltage (295.4V) to the simulated LTSPICE reading (283.5V). The discrepancy between the

theoretical and simulated values are expected, as the non-ideal parasitic behavior of the passive components in the LTSPICE were modeled after their real world counterparts.

The primary contributor to this voltage drop is the interaction between the Zener diode (BZX84C12L [25]) Gate protection and the high impedance 4-band RC-filter array. The filter introduced a 188kΩ of series resistance and the real world zener diodes exhibit reverse leakage current (I_R) operating below the assumed 4.0V Zener voltage. This current leakage, combined with the MOSFET's gate leakage, reduces the absolute measured voltage at the Gate.

This deviation of 11.9V is well within the Vacuum tube power rail requirements, as the Valve amplifiers usually operate from 100V+DC to 300V+DC power supplies.

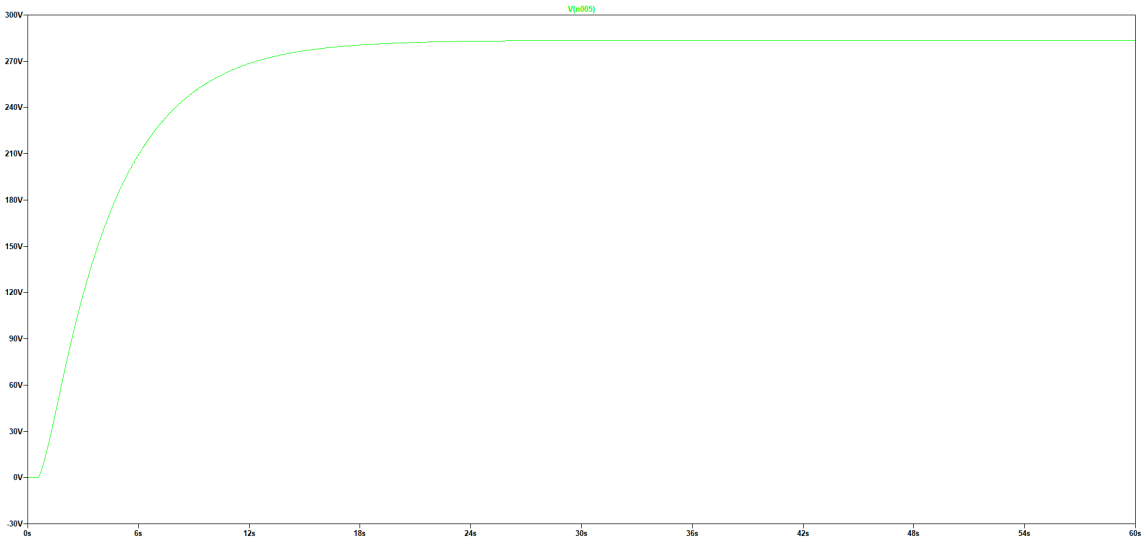


Figure 5: LTSPICE 280V PSU Voltage Readings

As shown in Figure 5, the slow-start function of the 4-band Capacitance Multiplier Circuit is working as intended, with smooth, gradual rise and non-existent overshoot, culminating in a flat, gentle line measured at 283.5V by the 60 second mark.

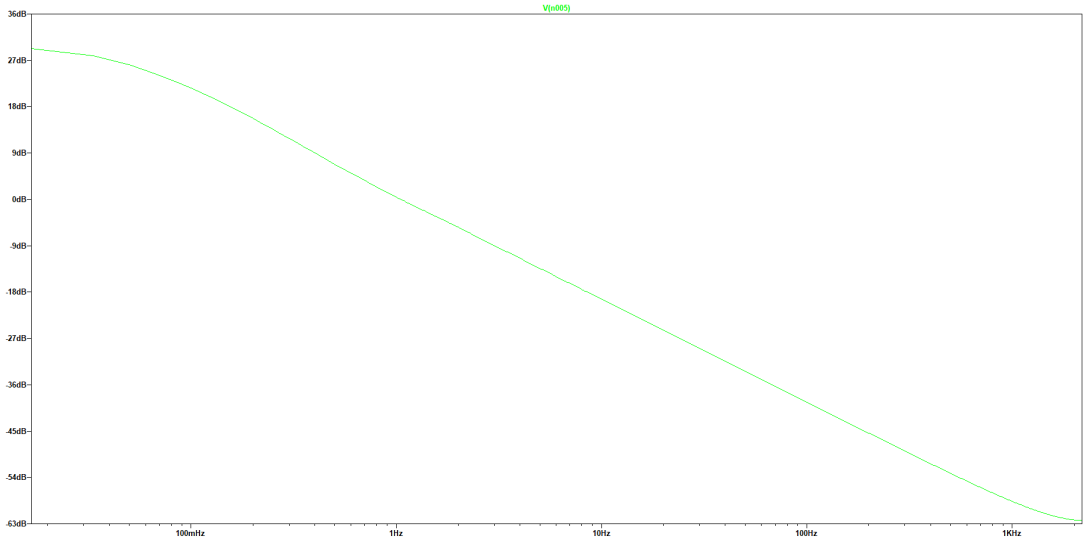


Figure 6: LTSPICE 280V PSU FFT Readings

Furthermore, the FFT analysis of the curve shows a straight downward sloping curve, with minimal ripples or oscillation.

3.2 The Version 2.0

With a sharp departure from the planned version number 1, highlighted by the difficulty of integrating a WiFi and Bluetooth-enabled MCU (ESP32-C3) into a mixed signal circuit: high voltage power lines (283V) on the same layer as the sensitive low voltage digital and analog power lines, high speed USB 2.0 data lines, high acquisition price of state-of-the-art components (ESS9039Q2M DAC, ADAU1467 DSP), three toroidal transformers for the clean power supply, and the CNC-milled for the aluminum case all made it financially and technically infeasible to build in the timeframe.

The bulky desktop architecture, with the simulation work highlighted here was scrapped in favor of a portable DAC/AMP: with the Comtrue CT7601CR MCU/USB hub in the heart, an independent master clock to supply clean signal to the MCU Phase-Locked Loop (PLL) to multiply and synthesize the 12MHz input to higher accepted frequencies , dual-mono low-power DAC/AMP chips (Cirrus Logic CS43131) [9], with two output ports: the industry standard 3.5mm unbalanced output (PJ-320D) and the audiophile standard 4.4mm balanced output (GT-3321667P-01), Electrostatic Discharge (ESD) protection diode (TPD2E001DZDR) [14], 16-pin USB 2.0 USB-C port [19] and SGM2036 LDOs [12] for the Power Distribution Network.

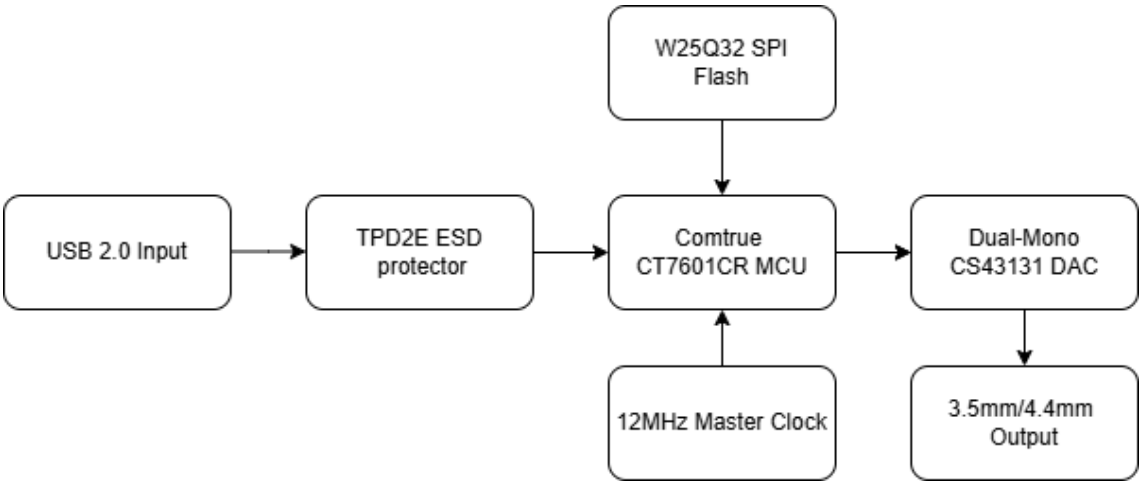


Figure 7: Architecture of the Version 2

The CT7601CR chip was chosen for several reasons: extensive use in high-performance Digital Audio Players (DAPs), Mid-to-High range Digital Analog Converter dongles and Devices (DACs), 32-bit/384kHz PCM playback support, low-power consumption (<250mA) in its two power inputs (3.3V and 1.2V), small form factor (QFN-48).

Cirrus Logic CS43131 widely adopted in the portable audio industry for its combination of performance and power efficiency: high-performance, low-power 32-bit stereo DAC with 2VRMS of output into 600Ω high-impedance headphones with an interchannel isolation of >110 dB, and 30 mW into 32 Ω low impedance headphones.. An integrated class H amplifier with adaptive power supply, proprietary AC detection system to identify the connected headphone and optimizes its output to maximize battery efficiency.

The addition of TPD2E001DZDR, a two-channel, low-capacitance Transient Voltage Suppressor (TVS) diode is designed to provide Electrostatic Discharge protection to the DN and DP USB data transmission lines.

Rated for IEC 61000-4-2 Level 4 ESD protection [20], handling up to 8kV contact discharge and 1.5kV air-gap discharge, features a typical I/O capacitance of 1.5pF, which made it the premier choice for the PCB protection role.

SGM2036 (300mA) LDOs were used extensively in the Power distribution network: providing stable power for all the components.

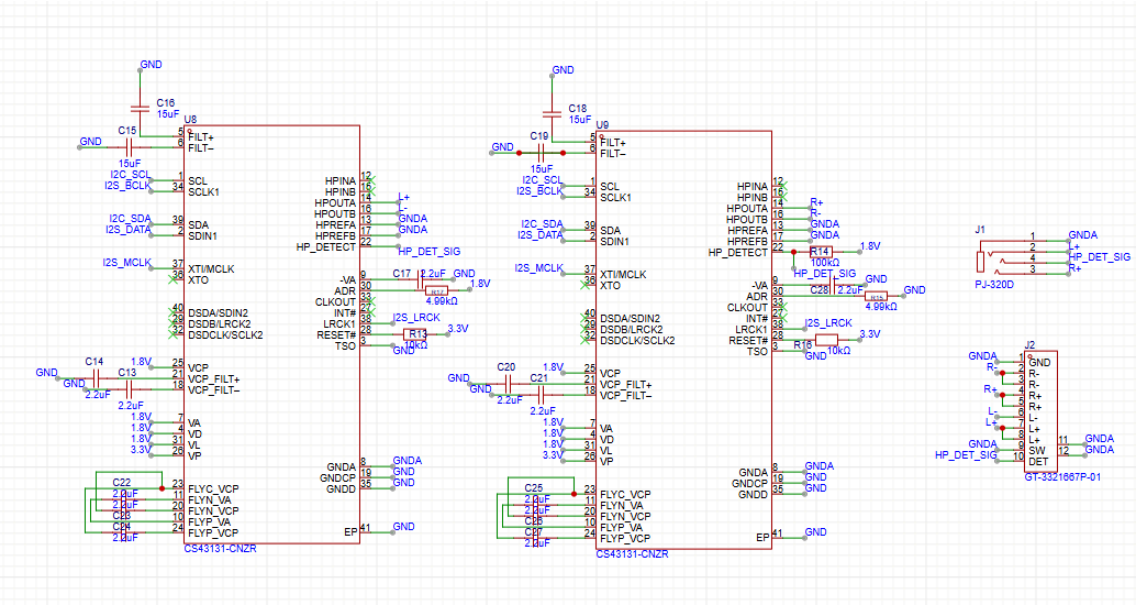


Figure 8: Analog stage schematics of the Version 2

This version of the thesis was extensively done in the schematics stage: planned triple ground polygons: general ground, analog ground, digital ground (GND, GNDA, GNDD) layer with the use of star grounding to minimize the crosstalk, single crystal oscillator to simplify the master clocks.

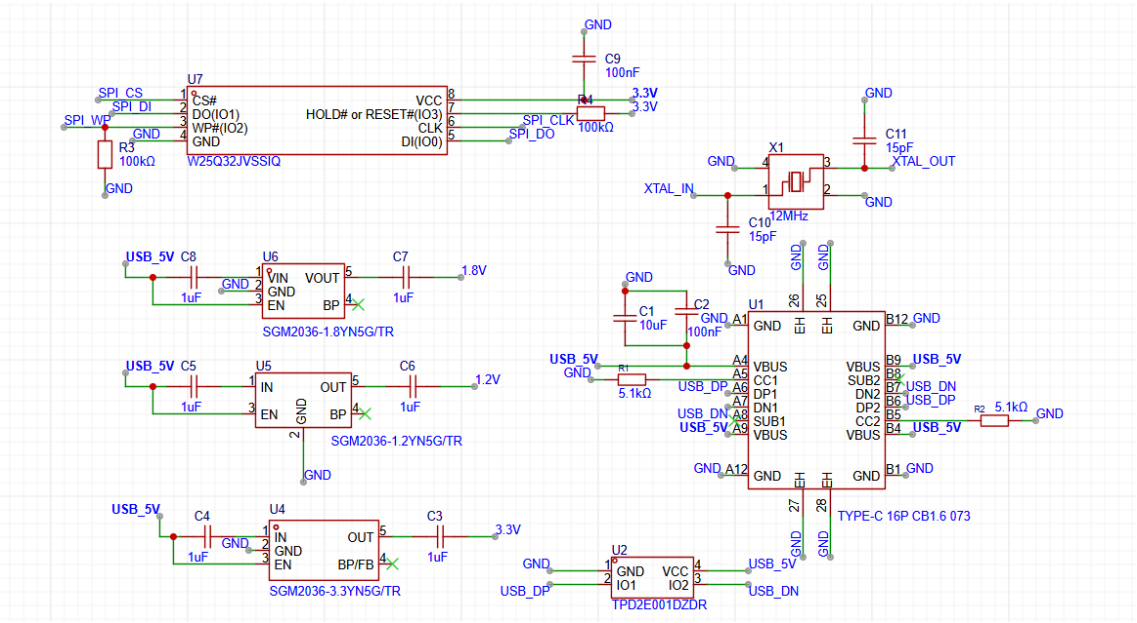


Figure 9: PDN/passive IC schematics of the Version 2

The use of passive components: bulk, decoupling capacitors, termination and pull-up resistors; followed the manufacturer stated values and placements. The use of preregulated LDOs minimized the form factor for the PCB routing.

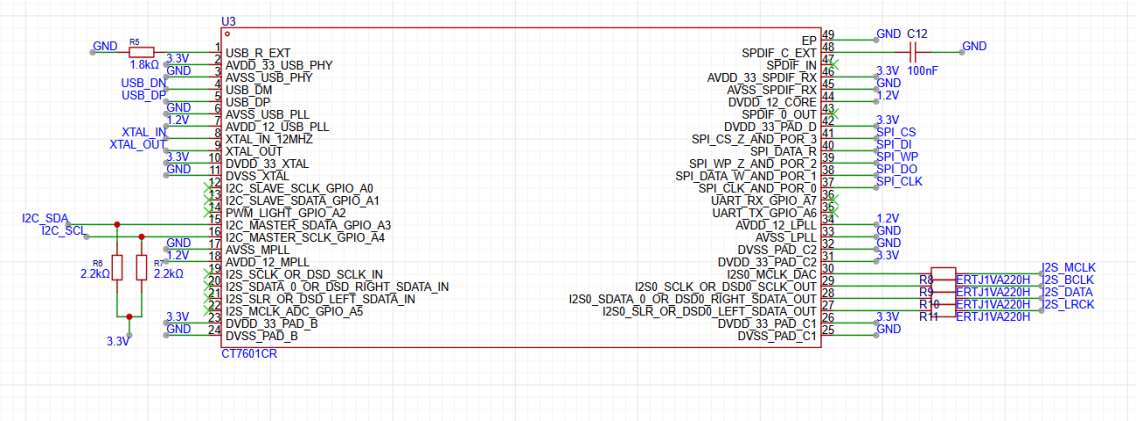


Figure 10: MCU schematics of the Version 2

The schematic for the CT7601CR was arguably the easiest to work with: the labeled pins, wide schematic gave it a very logical line of progression.

However, the second version had a fatal flaw: the manufacturer Comtrue of the used MCU does not provide an Integrated Development Environment (IDE), open-source code, nor a devkit. The use of .bin files for the firmware, coupled with their closed-source, proprietary development environment made it impossible to continue.

3.3 Version 2.0, the First Revision

Following the discovery of Comtrue's closed-source development environment, the CT7601CR was removed from the design and replaced with XMOS's XU208-128-TQ64 [8], a well-established asynchronous USB audio processor with a proven track record in high-end desktop and portable audio equipment.

The XU208 operates on XMOS's xCORE architecture: a deterministic multicore processor with eight logical cores running at up to 500 MIPS aggregate throughput, each capable of real-time signal processing without the latency uncertainty introduced by interrupt-driven microcontrollers. This determinism is critical in audio applications, where timing jitter in the digital domain directly translates to phase noise and THD+N degradation at the analog output.

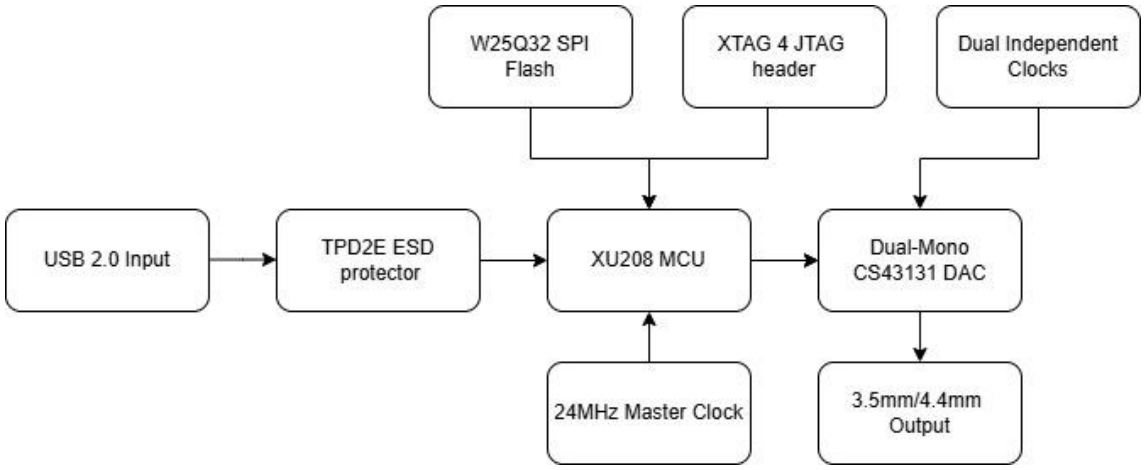


Figure 11: Architecture of version 2.0, revision 1

The chip integrates a full-speed and high-speed USB 2.0 PHY compliant with the USB Audio Class 2.0 (UAC2) standard [18], enabling bit-perfect PCM audio transmission at up to 32-bit/384kHz without proprietary drivers on macOS and Linux, and with freely available drivers on Windows. This open standard compliance was the decisive factor in the MCU replacement decision - unlike the CT7601CR, XMOS provides a fully open-source firmware stack (sc_usb_audio) [26], a dedicated development kit (xTIMEcomposer Studio / XMOS Tools), and an active developer community.

The XU208 operated from a single 3.3V rail with a 1.0V core supply, both provided by the SGM2036 LDOs of the Power Distribution Network, consuming under 150mA under typical audio streaming load.

3.4 Version 2.0, the Second Revision

3.4.1 XU208-128-TQ64-I10 MCU Schematic Analysis

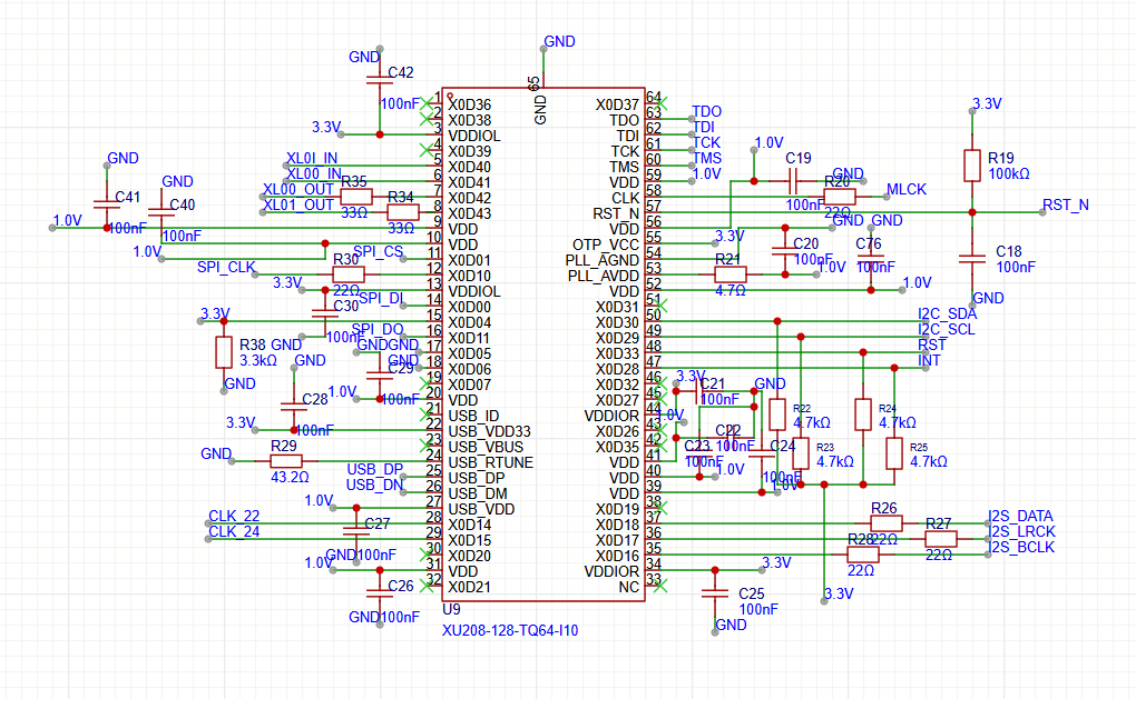


Figure 12: MCU configuration schematic of the Version 2 Revision 2

The schematic implementation of the XMOS XU208-128-TQ64-I10, shown in Figure 12, represents the most complex and signal-integrity-critical section of the Version 2, Second Revision design. The following analysis documents the design decisions made for each interface domain of the MCU, with particular attention to passive component selection and signal line treatment.

3.4.1.1 USB 2.0 Interface

The USB differential pair — USB_DP and USB_DN — connects directly to the XU208's integrated USB 2.0 PHY at pins 25 and 26 without external series termination resistors. The PHY's output driver impedance is calibrated internally using R29 (43.2Ω), connected from the RTUNE pin (24) to ground. This precision resistor provides the bias current reference from which the PHY derives and sets its driver output impedance to meet the USB 2.0 90Ω differential specification — the correct implementation per the XU208 hardware design guide [8], which specifies that external DP/DN termination is unnecessary when using the integrated PHY. Absent or incorrectly valued RTUNE

termination results in a miscalibrated PHY that fails to meet the USB 2.0 driver strength specification [19], degrading signal quality at the far end of the cable.

The USB_VBUS line at pin 23 is monitored by the XU208 for USB connection detection. TThe CLK_22 and CLK_24 net labels visible at the bottom left of the schematic are XU208 GPIO outputs routed to the STAND-BY pins of U10 (22.5792MHz) and U8 (24.576MHz) respectively. The XU208 firmware asserts the appropriate line to enable the oscillator matching the incoming stream's sample rate family — 44.1kHz content activates U10 via CLK_22, 48kHz content activates U8 via CLK_24 — while holding the unused oscillator in standby. The clock signal itself exits each oscillator on its output pin, passes through the 22Ω series termination resistor R18 or R17, and routes to the CS43131 XTI/MCLK inputs as the MLCKD net.

3.4.1.2 SPI Flash Interface

The W25Q32JVSSIQ serial flash connects to the XU208 via a four-wire SPI bus: SPI_CS, SPI_CLK, SPI_DI, and SPI_DO. R30 (22Ω) on the SPI_CS line provides source termination at the MCU output. R38 (3.3kΩ) pulls the SPI_CS line high, ensuring the flash remains deselected during the power-up interval before the XU208 asserts active-low chip select control — without this pull-up the CS line floats during startup, creating the possibility of spurious flash reads that corrupt the boot sequence. C30 (100nF) provides decoupling on the 3.3V supply local to the SPI interface, minimising supply impedance at SPI clock frequencies.

3.4.1.3 I2S Audio Output

The I2S bus — comprising I2S_DATA, I2S_LRCK, and I2S_BCLK — carries the digital audio stream from the XU208 to the dual CS43131 DAC chips. All three lines are fitted with 22Ω source termination resistors (R26, R27, R28) at the XU208 output. While I2S_DATA and I2S_LRCK operate at audio-rate frequencies, I2S_BCLK at maximum resolution operates at 384kHz × 64 bits = 24.576MHz — a frequency at which PCB traces exhibit transmission line behavior and unterminated lines produce measurable reflections. The 22Ω source resistors damp these reflections at the driver output without attenuating the signal amplitude at the receiver to a degree that violates the CS43131 input logic thresholds. The MLCK master clock output carries a 22Ω series termination resistor (R20) by the same reasoning, maintaining consistent signal integrity treatment across all high-frequency outputs of the MCU.

3.4.1.4 I2C Configuration Bus

The I2C bus provides the XU208 with a runtime configuration interface to both CS43131 DAC chips, enabling control of output volume, output mode selection between single-ended and balanced, and headphone impedance detection response. Four 4.7kΩ pull-up resistors are present across the I2C_SDA and I2C_SCL lines — R22 and R24 on I2C_SDA, R23 and R25 on I2C_SCL — one pull-up per device per line, consistent with the standard topology for a two-device I2C bus with two independently addressed CS43131 chips. The RST and INT lines provide hardware reset and interrupt signalling between the XU208 and the CS43131 devices, allowing the MCU firmware to manage DAC initialisation sequencing and headphone insertion events deterministically.

The xCORE logical I/O ports — XL00_IN, XL00_OUT, XL01_IN, XL01_OUT — are protected by 33Ω current-limiting resistors (R34, R35). These ports are the XU208's general-purpose deterministic I/O, used for GPIO functions within the firmware. The resistors protect the xCORE port drivers from overcurrent in the event of bus contention or an external fault condition.

3.4.1.5 Power Supply Decoupling Strategy

The decoupling network across the XU208's supply pins represents one of the most carefully considered aspects of the schematic. The chip operates from two supply domains — 3.3V for the I/O ring and 1.0V for the digital core — each decoupled independently at every supply pin with 100nF ceramic capacitors placed as close to the pin as physically achievable. This distributed decoupling strategy ensures that high-frequency transient currents drawn by switching logic are sourced locally from the capacitor charge rather than travelling along the supply trace from the regulator, which would produce a voltage drop proportional to the trace inductance and the rate of current change.

The PLL_AVDD supply pin receives dedicated, isolated decoupling treatment. The XU208's internal PLL generates the I2S master clocks synthesised from the 24MHz reference oscillator input, and any supply noise on PLL_AVDD modulates the VCO control voltage directly — manifesting as phase noise on the output clock and consequently as jitter at the DAC input. The 4.7Ω resistor R21 forming an RC filter between the digital supply and PLL_AVDD, combined with the dedicated decoupling

capacitors C20 and C76 on this pin, provides supply domain isolation within the chip's own power network..

The GND_AGND pin provides the XU208's internal PLL with a dedicated analog ground reference. Its connection to the board's unbroken ground plane, rather than a split analog ground polygon, is consistent with the ground plane philosophy discussed previously: a continuous low-impedance return path for all currents, with subsystem isolation achieved through placement rather than plane splitting.

The RST_N line is pulled high to 3.3V through R19 (100kΩ), ensuring the XU208 remains out of reset under normal operating conditions while allowing the JTAG debug host to assert a clean logic-low reset without fighting a low-impedance pull. The JTAG debug interface — TDO, TDI, TCK, TMS, and TRST — is fully exposed in the schematic, providing access to the XU208's on-chip debug infrastructure through xTIMEcomposer Studio for setting breakpoints, inspecting core state, and verifying I2S timing against the CS43131 input requirements.

3.4.2 CS43131-CNZR Dual-Mono Analog Stage Schematic Analysis

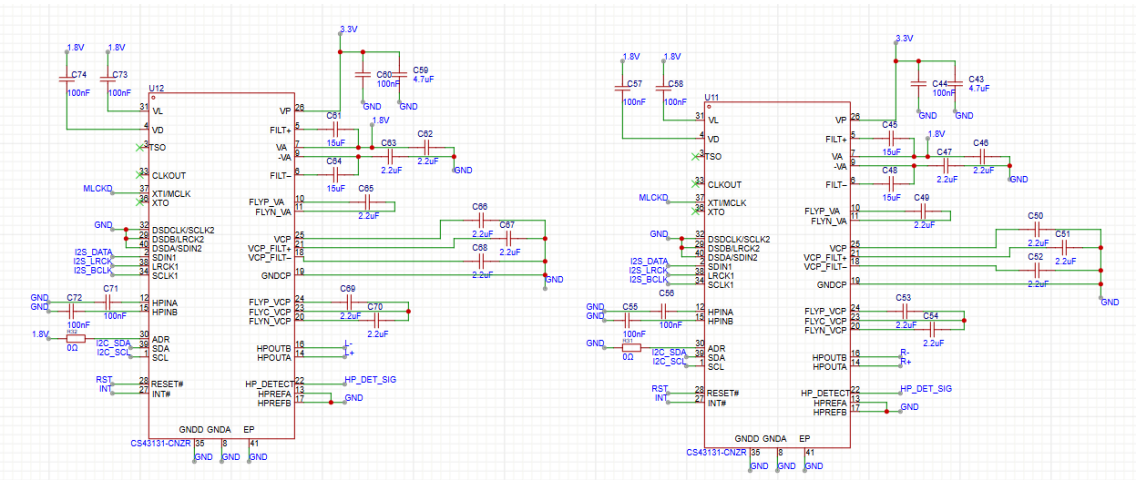


Figure 13: DAC configuration schematics of the Version 2 Revision 2

The analog output stage, shown in Figure 13, implements a true dual-mono architecture using two independent CS43131-CNZR devices — one assigned to the left channel and one to the right. This topology, borrowed from high-end desktop audio

design, provides complete physical separation of the two audio channels at the DAC level, eliminating the interchannel crosstalk that arises when a single stereo DAC shares its analog output stage between channels. The CS43131's specified interchannel isolation of greater than 110dB [9] is a per-chip figure; the dual-mono implementation ensures this specification applies to the complete signal path rather than just the DAC core.

3.4.2.1 I2S Digital Input Interface

Each CS43131 receives its own dedicated I2S feed from the XU208. The three-wire bus — I2S_DATA, I2S_LRCK, and I2S_BCLK — routes independently to each chip, with DSDA/SDIN carrying the audio data, DSDCLK/LRCK carrying the left-right word clock, and DSDB/SCLK carrying the bit clock. The separate SDIN1 and SDIN2 inputs on each chip confirm that the XU208 is configured to drive each DAC independently rather than daisy-chaining a single I2S stream — a more demanding firmware configuration that eliminates any shared digital path between channels.

The XTI/MCLK input on each CS43131 receives its dedicated master clock — 22.5792MHz for 44.1kHz family content and 24.576MHz for 48kHz family content — directly from the independent crystal oscillators discussed in the clock architecture section. These frequencies are exact 512× multiples of their respective sampling families; supplying the DACs with a dedicated, pre-synthesised clock rather than a PLL-derived signal eliminates accumulated phase noise from clock multiplication, directly improving jitter performance at the DAC input and consequently the THD+N of the analog output. The CLKOUT pin is also exposed, providing a buffered clock reference available to downstream circuitry if required.

3.4.2.2 Class H Charge Pump Network

The most visually distinctive feature of the CS43131 schematic is the extensive flying capacitor network surrounding each chip. The CS43131 integrates a Class H amplifier with an adaptive charge pump that dynamically scales the headphone amplifier supply voltage to match the instantaneous output level — rather than maintaining a fixed supply rail, which would dissipate excess power as heat at low output levels, the Class H architecture switches between supply levels in real time, reducing power consumption during quiet passages while maintaining full voltage headroom for peaks.

The charge pump requires a network of flying capacitors to generate and switch between its internal supply levels. On each chip, the VCP and VCP_FILT+/− pins carry 2.2µF flying capacitors forming the positive charge pump reservoir, bootstrapping the amplifier supply above the 1.8V input rail to provide sufficient headroom for the output stage. The FLYC_VCP and FLYN_VCP pins carry the flying capacitors that transfer charge between voltage levels; the 2.2µF value is specified in the CS43131 application note [9], and deviating from it affects the charge pump switching frequency and output ripple characteristics. The FILT+ pin with 15µF capacitors provides supply filtering for the amplifier output stage, acting as a local energy reservoir that supplies instantaneous current during output transients without drawing from the main supply rail, reducing supply-coupled distortion at the output.

3.4.2.3 Headphone Output and Detection

The HPOUTA and HPOUTB pins on each chip provide the differential headphone output signals. The two output pins per chip represent the positive and negative phases of a fully differential output, enabling both single-ended operation through the 3.5mm TRS jack and balanced operation through the 4.4mm Pentaconn connector. In single-ended mode HPOUTB serves as a driven virtual ground; in balanced mode both phases carry equal and opposite signal components, providing 6dB of additional voltage swing and common-mode noise rejection at the headphone driver.

The HP_DETECT and HP_DET_SIG lines implement the CS43131's headphone detection system. On insertion, the detection circuitry measures the impedance of the connected load and signals the XU208 via the INT interrupt line, allowing the firmware to configure the CS43131's output stage for the detected impedance — maximising output voltage for high-impedance loads and limiting current for low-impedance loads. The HPREFA and HPREFB pins are terminated to GNDA, ensuring the amplifier reference is derived from the analog ground domain rather than the noisier digital ground.

3.4.2.4 I2C Address and Configuration

The ADR pin on each CS43131 sets the chip's I2C device address, allowing both chips to coexist on the same bus with distinct addresses for independent firmware control. U12 (right channel) has its ADR pin pulled to 1.8V through a 0Ω resistor,

assigning it the high address, while U11 (left channel) has its ADR pin pulled to GND, assigning it the low address. The XU208 firmware uses these distinct addresses to configure each chip independently — setting volume, output mode, and detection thresholds per channel without conflict.

The RST and INT pins provide hardware reset and interrupt capability. The RST line allows the XU208 to perform a hard reset of each DAC independently during initialisation, ensuring a known register state before audio playback begins. The INT line signals the XU208 when a headphone insertion or removal event occurs, triggering the impedance detection routine.

3.4.2.5 Supply Decoupling Architecture

Each CS43131 operates from the 1.8V rail generated by the SGM2036 downstream of the TPS7A9101 cascaded regulator. The supply decoupling on each chip follows a two-tier strategy: 100nF bulk capacitors on the VP supply pin handle mid-frequency transients, while the charge pump filter capacitors handle the high-frequency demands of the switching amplifier stage. The GNDD and GNDA pins on each chip connect to the board's unbroken ground plane, confirming that the CS43131's internal ground domain separation is respected at the chip boundary while maintaining a single continuous return path at the board level. The exposed pad on each chip provides the primary thermal and electrical ground connection for the QFN package and connects directly to the ground plane through multiple vias in the PCB layout.

3.4.3 Power Distribution Network and USB Interface Schematic Analysis

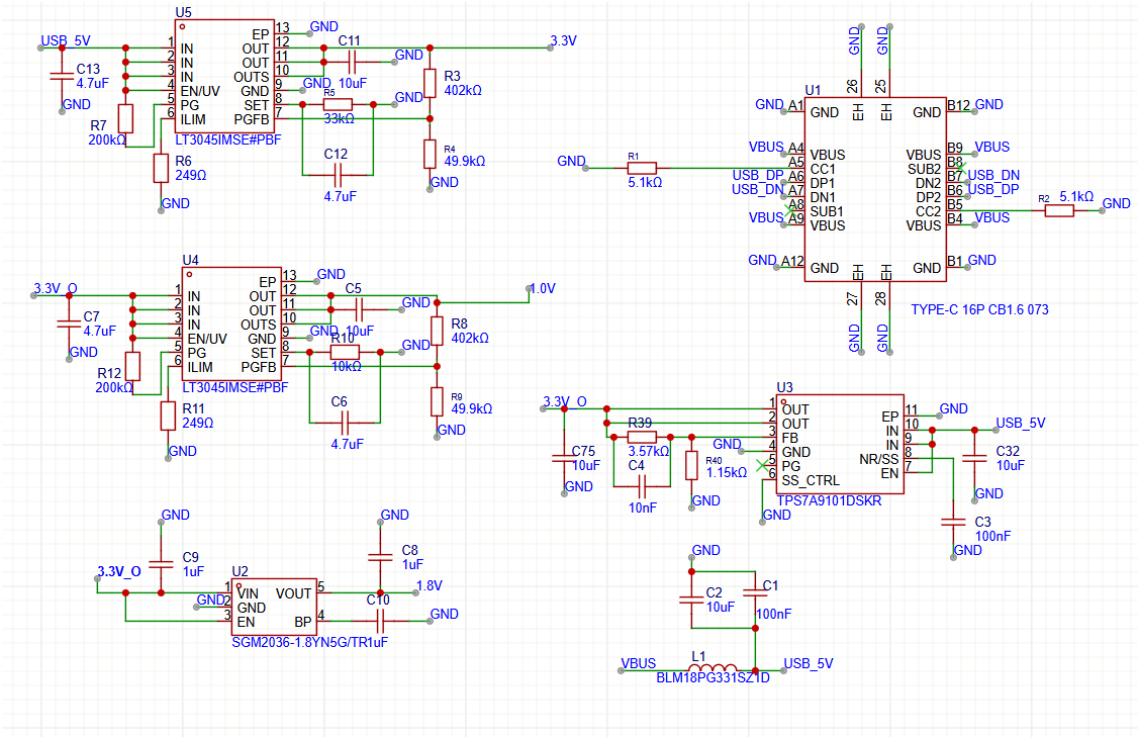


Figure 14: PDN and USB interface schematics of the Version 2 Revision 2

The PDN and USB interface schematic, shown in Figure 14, documents the complete power delivery architecture of the Version 2, Second Revision. This page contains five distinct functional blocks: two LT3045 ultra-low-noise regulators, the SGM2036 1.8V LDO, the TPS7A9101 regulator, the USB-C receptacle with CC line handling, and the TPD2E001DZDR ESD protection device. Together these form the complete power and USB front-end of the design.

3.4.3.1 Voltage Cascading Architecture

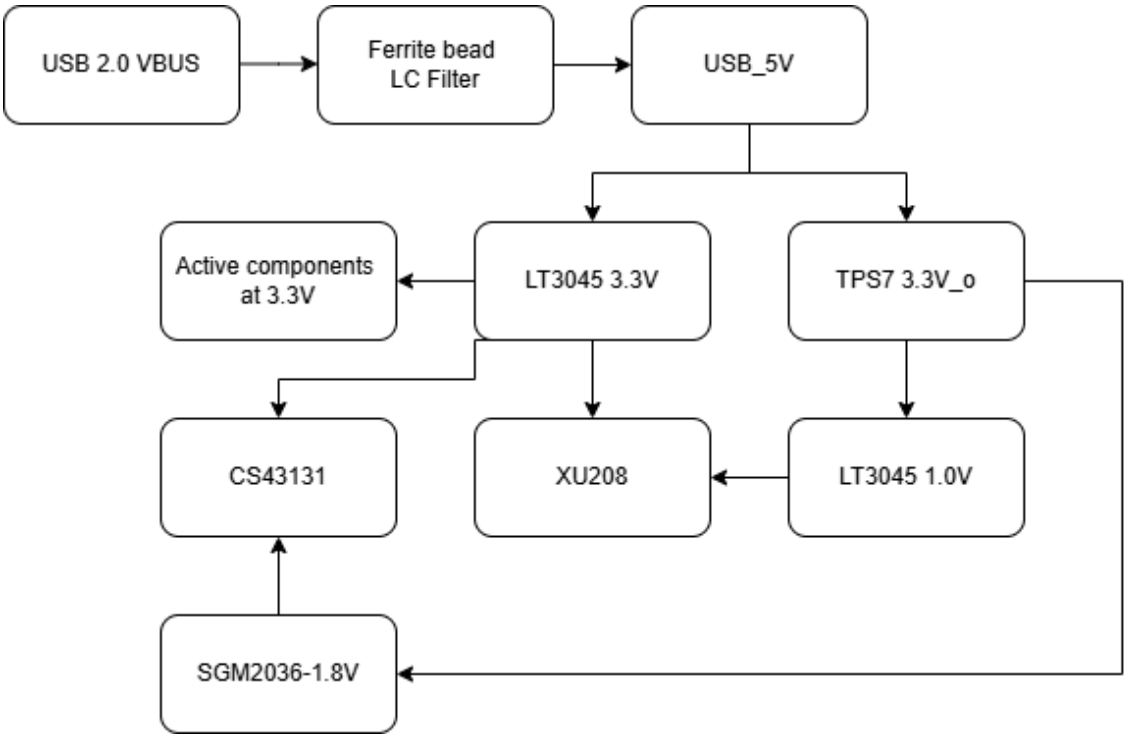


Figure 15: PDN architecture of the Version 2 Revision 2

The PDN employs a multi-stage cascaded regulation strategy. Raw VBUS from the USB-C connector passes through the BLM18PG331SZ1D ferrite bead L1 and the bulk input filter capacitors C2 (10µF) and C1 (100nF), becoming the USB_5V net. This feeds two parallel first-stage regulators from the USB_5V net: U5 LT3045, generating the 3.3V digital logic rail directly from USB_5V, and U3 TPS7A9101, generating the 3.3V_O conditioned rail. The TPS7A9101 drives its own feedback network independently and operates in parallel with U5 rather than in series with it. U3's 3.3V_O output then feeds the downstream noise-critical chain: U4 LT3045 generating the 1.0V core supply for the XU208, and U2 SGM2036 generating the 1.8V supply for the CS43131 DAC chips. This topology provides two stages of cascaded noise rejection between USB_5V and the analog supply rails — the TPS7A9101's 4.4µV RMS output noise feeding into the downstream LT3045 and SGM2036 — while the 3.3V digital logic rail is served directly by U5 LT3045 from USB_5V without the intermediate TPS7A9101 conditioning stage.

3.4.3.2 LT3045 Dual Regulator Instances (U4, U5)

Two LT3045IMSE#PBF [10] instances are present. U5 generates the 3.3V digital logic rail directly from USB_5V, supplying the XU208 I/O ring and all active components operating at 3.3V — including the crystal oscillators U8, U10, and U13, the W25Q32JVSSIQ SPI flash U7, and the JTAG header logic level. U4 generates the 1.0V XU208 core supply from the TPS7A9101's conditioned 3.3V_O rail. The two instances therefore serve distinct roles in the PDN hierarchy: U5 is a direct first-stage regulator from USB_5V for digital logic loads, while U4 is a second-stage regulator in the noise-critical cascade chain serving the XU208 core exclusively

The SET pin on each LT3045 programs the output voltage through the relationship V_OUT = I_SET × R_SET, where I_SET is an internal precision current source. U5 (3.3V output) uses R5 (33kΩ) while U4 (1.0V output) uses R10 (10kΩ). The PGFB pin on each device connects to a resistor divider — R3 (402kΩ) and R4 (49.9kΩ) on U5, R8 (402kΩ) and R9 (49.9kΩ) on U4 — setting the power-good threshold at approximately 90% of the nominal output voltage. The OUTS pin on each device connects through R6 (249Ω) on U5 and R11 (249Ω) on U4, setting the output current sense threshold for each regulator's overcurrent protection. The ILIM pin on each device is set by R7 (200kΩ) on U5 and R12 (200kΩ) on U4, programming the current limit appropriate for the expected load of each rail.

Each LT3045 instance is decoupled with a 4.7µF output capacitor (C12 on U5, C6 on U4) and a 10µF output sense capacitor (C11 on U5, C5 on U4). The 4.7µF input bypass capacitors (C13 on U5, C7 on U4) suppress input voltage transients that could couple through to the output and degrade the regulator's PSRR performance. The EN/UV pins on both devices are tied to their respective input rails, ensuring the regulators are permanently enabled once supply voltage is present.

3.4.3.3 TPS7A9101DSKR (U3)

The TPS7A9101DSKR [11] takes USB_5V as its input and generates the 3.3V_O conditioned rail that supplies all noise-sensitive downstream loads. The feedback network uses the manufacturer's recommended resistor values for a 3.3V output — R39 (3.57kΩ) and R40 (1.15kΩ) — programming the output through the FB pin per the TPS7A9101 application note. The TPS7A9101 features an ultralow noise

output of 4.4μV RMS, making it well suited as the upstream conditioner for the DAC and MCU core power chain.

The NR/SS pin with capacitor C4 (10nF) implements soft-start, controlling the output voltage ramp rate during power-up to prevent inrush current from collapsing the USB_5V rail. The SS_CTRL net label on the NR/SS pin confirms this soft-start timing is a deliberate design parameter. The EN pin is tied to USB_5V, permanently enabling the device once VBUS is present.

3.4.3.4 SGM2036-1.8YN5G/TR (U2)

The SGM2036 [12] generates the 1.8V rail for the CS43131 DAC chips from the TPS7A9101's conditioned 3.3V_O output. The output delivers 1.8V with C10 (1μF) for output stability and C9 (1μF) as input bypass. The BP pin with bypass capacitor C8 (1μF) provides internal bandgap reference filtering, reducing the contribution of reference noise to the output noise floor. The EN pin is tied high, permanently enabling the device. The cascade topology — TPS7A9101 conditioning stage feeding the SGM2036 — provides two stages of noise rejection before the 1.8V supply reaches the CS43131 analog supply pins, appropriate for a 32-bit audio converter.

3.4.3.5 USB-C Receptacle (U1 — TYPE-C 16P CB1.6 073)

The USB-C connector implements the standard device-side connection. The CC1 and CC2 configuration channel lines are pulled down through R1 and R2 (both 5.1kΩ) to ground — the USB-C specification value for a device (UFP) to signal its presence to a host and initiate power delivery negotiation. The SuperSpeed USB 3.0 signal pins (SUB1, SUB2, DN1, DN2, DP1, DP2) are left unconnected, consistent with a USB 2.0 only design — only the USB_DP and USB_DN differential pair is used for data. Multiple VBUS pins on both sides of the connector body are shorted together to distribute current and reduce contact resistance under load. The USB_DP and USB_DN lines route to the TPD2E001DZDR ESD protection device before reaching the XU208 MCU — connector, then ESD protection, then MCU — ensuring transient voltages are clamped before they reach the MCU input.

3.4.4 Peripheral and Interface Schematic Analysis

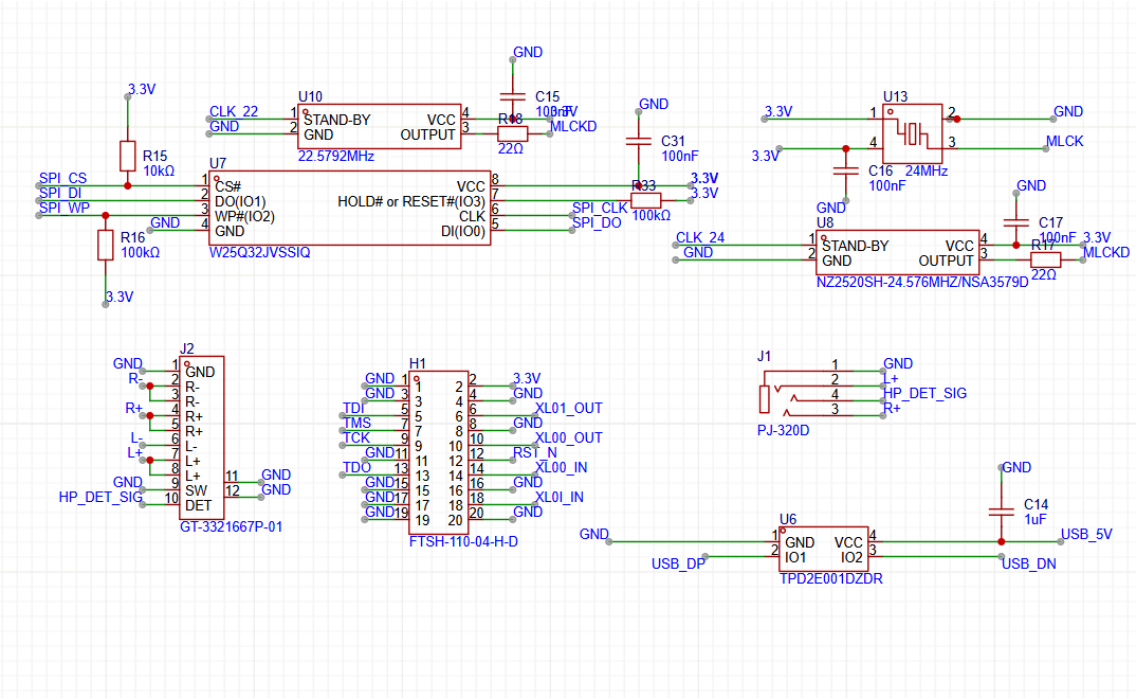


Figure 16: Peripheral and Interface schematics of the Version 2 Revision 2

The peripheral schematic, shown in Figure 16, documents the remaining functional blocks of the Version 2, Second Revision: the VBUS input filtering, SPI flash memory, dual audio output connectors, three independent clock oscillators, the JTAG debug header, and the 24MHz master reference clock. Together these complete the signal chain from USB input to analog output jack.

3.4.4.1 VBUS Input Filter — BLM18PG331SZ1D (L1)

The raw VBUS line from the USB-C connector passes through a BLM18PG331SZ1D ferrite bead (L1) [15] before becoming the USB_5V net that feeds the TPS7A9101 conditioning stage. The BLM18PG331SZ1D presents 330Ω impedance at 100MHz — chosen specifically to suppress high-frequency switching noise on the USB VBUS line without introducing significant DC resistance that would cause voltage drop under load. The ferrite bead presents negligible impedance at DC and low frequencies, preserving the full VBUS voltage for the downstream regulators, while attenuating MHz-range noise generated by the host's switching power supply before it enters the board's power domain.

The two-capacitor input filter — C2 (10µF) and C1 (100nF) in parallel — forms the second element of the input filter network. The 10µF bulk capacitor handles low-frequency transients and provides charge storage during load steps, while the 100nF ceramic capacitor handles high-frequency noise above the ferrite bead's effective range. Together with L1, these three components form a broadband π-filter at the board's power entry point — the first line of defence in the noise attenuation chain before the TPS7A9101 conditioner.

3.4.4.2 W25Q32JVSSIQ SPI Flash (U7)

The W25Q32JVSSIQ [13] is a 32Mbit serial NOR flash device storing the XMOS sc_usb_audio firmware image. It connects to the XU208 via SPI_CS, SPI_DI, SPI_WP, SPI_CLK, and SPI_DO. Three notable passive components are present:

R15 (10kΩ) on the CS# pin provides a pull-up to 3.3V, ensuring the flash remains deselected during power-up before the XU208 takes control of the SPI bus — a floating CS# line during startup creates the possibility of spurious flash access that corrupts the boot sequence. R16 (100kΩ) on the WP# pin pulls it high, permanently disabling hardware write protection and allowing in-field firmware updates over the SPI bus if required. R33 (100kΩ) on the SPI clock line provides a pull-up ensuring a defined idle state on the clock line between transactions. C31 (100nF) provides local high-frequency supply decoupling at the oscillator output stage immediately adjacent to the MLCKD net.

3.4.4.3 3.5mm Headphone Output: PJ-320D (J1)

The PJ-320D is a through-hole 3.5mm stereo jack implementing the standard TRS unbalanced output. Its pinout connects pin 1 to GND, pin 2 to L+, and pin 3 to R+. The HP_DET_SIG line connects to pin 4 — the mechanical switch contact inside the jack that changes state when a plug is inserted. This signal routes to the CS43131 HP_DETECT input, triggering the chip's impedance detection routine on insertion and allowing the firmware to configure the output stage appropriately for the connected headphone load.

3.4.4.4 4.4mm Balanced Output: GT-3321667P-01 (J2)

The GT-3321667P-01 is a 4.4mm Pentaconn balanced output connector providing five signal contacts: L+, L−, R+, R−, and ground. The Pentaconn connector implements a dual-contact design for each signal pole — two pins per signal — reducing effective contact resistance under load. All four signal connections route directly to the CS43131 differential output pins — HPOUTA and HPOUTB from the left channel chip to L+ and L−, and the equivalent outputs from the right channel chip to R+ and R−.

The balanced output topology provides two distinct advantages over the single-ended 3.5mm output. First, it doubles the available output voltage swing — the CS43131 delivers 2VRMS from each output pin, giving 4VRMS differential across the load — sufficient to drive demanding planar magnetic headphones to reference listening levels. Second, the differential signal path provides common-mode noise rejection: any noise coupling equally onto both signal lines is cancelled at the headphone driver, leaving only the intended audio signal. The SW and DET pins implement the connector's insertion detection, with HP_DET_SIG shared with the 3.5mm jack detection circuit, allowing the firmware to determine which output is active and configure the CS43131 output routing accordingly.

3.4.4.5 Dual Audio Master Clocks — NZ2520SH-24.576MHz (U8) and 22.5792MHz (U10)

The two audio master clock oscillators occupy the right centre of the schematic. NZ2520SH-series [16] and NZ2520SDA-series [17] oscillators selected for their low phase noise, fast startup, and stable frequency output across the operating temperature range. U8 generates 24.576MHz and U10 generates 22.5792MHz — the exact 512× multiples of the 48kHz and 44.1kHz sampling families respectively. The active oscillator's output routes directly to the CS43131 XTI/MCLK inputs without passing through the XU208, preserving the clean, jitter-free signal that a direct crystal oscillator connection provides. Oscillator selection is managed by the XU208 via the CLK_22 and CLK_24 GPIO lines driving the STAND-BY pins of U10 and U8 respectively — only the oscillator matching the active sample rate family is enabled at any time, eliminating the potential for inter-oscillator interference and reducing idle power consumption

3.4.4.6 24MHz Reference Clock — U13

The 24MHz master reference clock for the XU208 PLL is implemented as a standalone active crystal oscillator. U13 outputs the MLCK net directly into the XU208 XTAL_IN input, with C16 (100nF) providing local supply decoupling at the oscillator VCC pin. The use of an active oscillator rather than a passive crystal is a deliberate noise management decision — a passive crystal requires the XU208's internal oscillator circuit to drive it, an active circuit whose noise contributes directly to the reference clock phase noise and therefore to the PLL output jitter. An active oscillator presents a low-impedance, already-buffered clock signal to the XU208 input, decoupling the reference clock quality from the XU208's internal oscillator noise floor.

3.4.4.7 JTAG Debug Header — FTSH-110-04-H-D (H1)

The FTSH-110-04-H-D is a 20-pin SMD debug header providing full JTAG access to the XU208's on-chip debug infrastructure. The header exposes TDI, TMS, TCK, TDO, and the xCORE logical I/O ports XL00_IN, XL00_OUT, XL01_IN, XL01_OUT, and RST_N — providing complete firmware debug capability through xTIMEcomposer Studio without requiring the board to be removed from its enclosure. The multiple dedicated GND pins distributed throughout the header pinout minimize loop area on each signal pin at JTAG clock frequencies, ensuring the debug interface does not compromise the board's ground integrity during active debugging sessions. The RST_N line allows the debug host to assert a hardware reset of the XU208 independently of the firmware — essential when debugging startup sequences or recovering from firmware states that prevent normal USB enumeration.

3.4.4.8 TPD2E001DZDR (U6)

The TPD2E001DZDR[14] sits electrically between the USB-C connector and the XU208 MCU, with its two I/O channels connected directly to USB_DP and USB_DN. During normal operation the device presents only its 1.5pF I/O capacitance to the signal lines with no effect on data transmission. During an ESD event its internal TVS diodes clamp the line voltage to a safe level within nanoseconds, diverting discharge current to the VCC and GND rails before it can reach the XU208's USB PHY input. C14 (1µF) on the USB_5V supply ensures the device has a stable local supply reference during clamping events, preventing the VCC pin from being pulled below ground during a negative ESD transient.

3.5 PCB Design

3.5.1 PCB Layout and Physical Implementation

The Version 2, Second Revision PCB layout, shown in Figure 14, represents the physical realisation of every design decision documented in the preceding sections. The board was fabricated as a 4-layer mixed-signal PCB through JLCPCB with a carefully considered layer assignment that prioritises signal integrity and power distribution simultaneously. The final board architecture was successfully routed within a compact 111.36 mm* 46.1 mm footprint

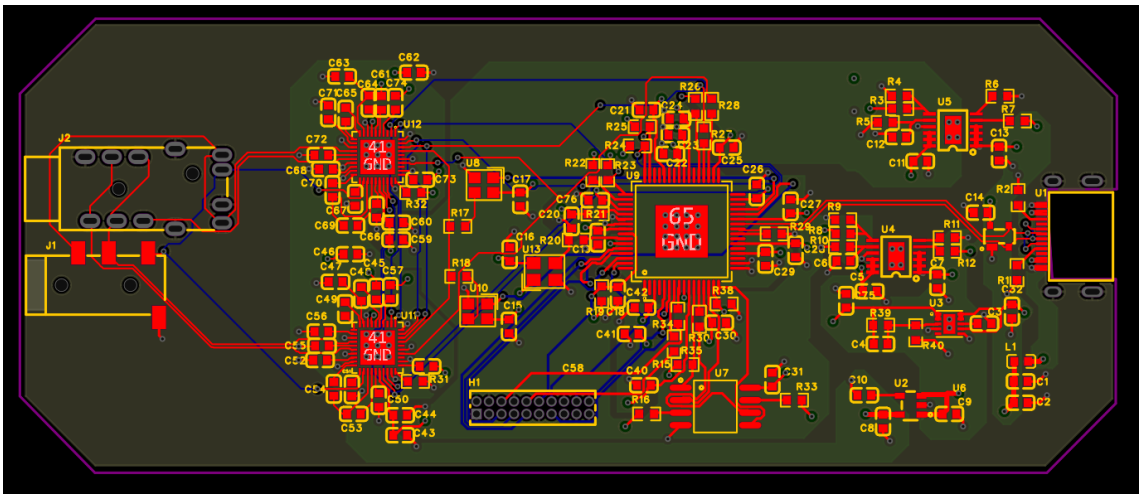


Figure 17: PCB CAD of the Version 2, Revision 2

3.5.2 4-Layer Stackup Architecture

The layer assignment follows established mixed-signal PCB practice for controlled impedance designs:

The Top Layer carries all high-speed and high-value signals — the USB differential pair, I2S audio bus, SPI flash interface, and master clock distribution traces.

Concentrating the fastest signals on the top layer minimizes via transitions on the critical signal paths, each of which introduces an impedance discontinuity and parasitic capacitance that degrades signal integrity at the operating frequencies involved.

Inner1 is dedicated entirely to an unbroken ground plane. Its position immediately adjacent to the Top Layer is deliberate — the return current for every top-layer signal flows on Inner1 directly beneath the signal trace, minimizing the area of the current loop formed by the signal and its return. Loop area is directly proportional to radiated EMI and to the inductance of the return path. Placing the ground reference as close as physically possible to the signal layer — separated only by the prepreg dielectric — minimizes both simultaneously. This is the stackup geometry recommended by IPC-2141A for controlled impedance mixed-signal designs [21].

Inner2 implements the power distribution network as a hierarchy of copper polygons. The VBUS polygon enters from the USB-C connector at the right board edge, transitions to USB_5V following the BLM18PG ferrite bead and bulk capacitor input filter, then branches into the 3.3V, 3.3V_O, 1.8V, and 1.0V regulated rails as each LDO generates its respective output. The polygon fills the entire available copper area of Inner2 not occupied by signal via clearances, providing the lowest possible impedance power distribution across each rail.

The Bottom Layer carries slower and lower-value signals — I2C configuration bus, GPIO, reset lines, interrupt signals, and headphone detection routing. Separating these low-frequency control signals from the high-speed audio and clock signals on the Top Layer eliminates the possibility of crosstalk between the two signal classes through shared routing layers.

3.5.3 Board Form Factor

The board outline implements a chamfered octagonal profile — a deliberate departure from the standard rectangular outline used in most prototype PCBs. The chamfered corners reduce the likelihood of PCB edge damage during handling and assembly, and present a product-appropriate form factor consistent with a portable audio device intended to sit alongside a digital audio player. The overall dimensions accommodate the full component density demanded by the dual-mono architecture while remaining compact enough for a portable dongle enclosure.

3.5.4 LT3045 3.3V Regulator Layout — U5

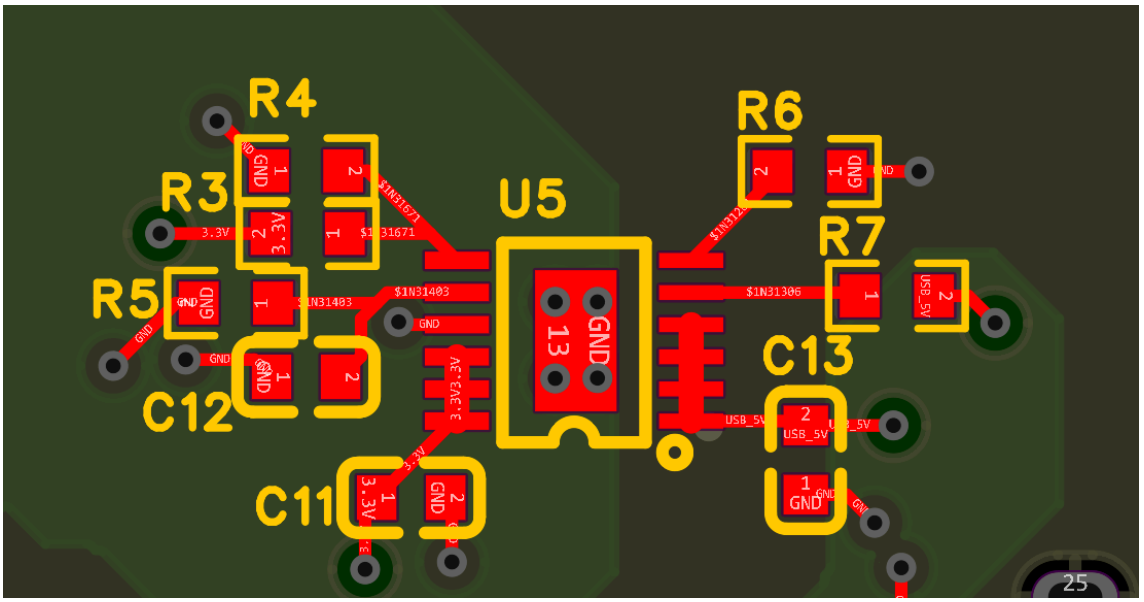


Figure 18: U5 LT3045 close-up

The LT3045 generating the 3.3V rail is shown in Figure 18 with its complete passive network. The feedback resistors R3, R4, and R5 form a tight cluster immediately around the SET and PGFB pins — minimising the loop area of the feedback network and the susceptibility of the output voltage setpoint to noise pickup. The output capacitors C11 and C12 are placed directly adjacent to the output pin, connected by the shortest possible trace segment. C13 provides an input bypass on the opposite side of the package.

The thermal pad ground vias on the U5 - visible as the circular grey pads — stitch the exposed thermal pad through to the Inner1 ground plane at multiple points, providing both the low-impedance electrical ground reference that the LT3045's PSRR depends upon and the thermal dissipation path for the package's power dissipation

3.5.5 PDN and USB Interface Region

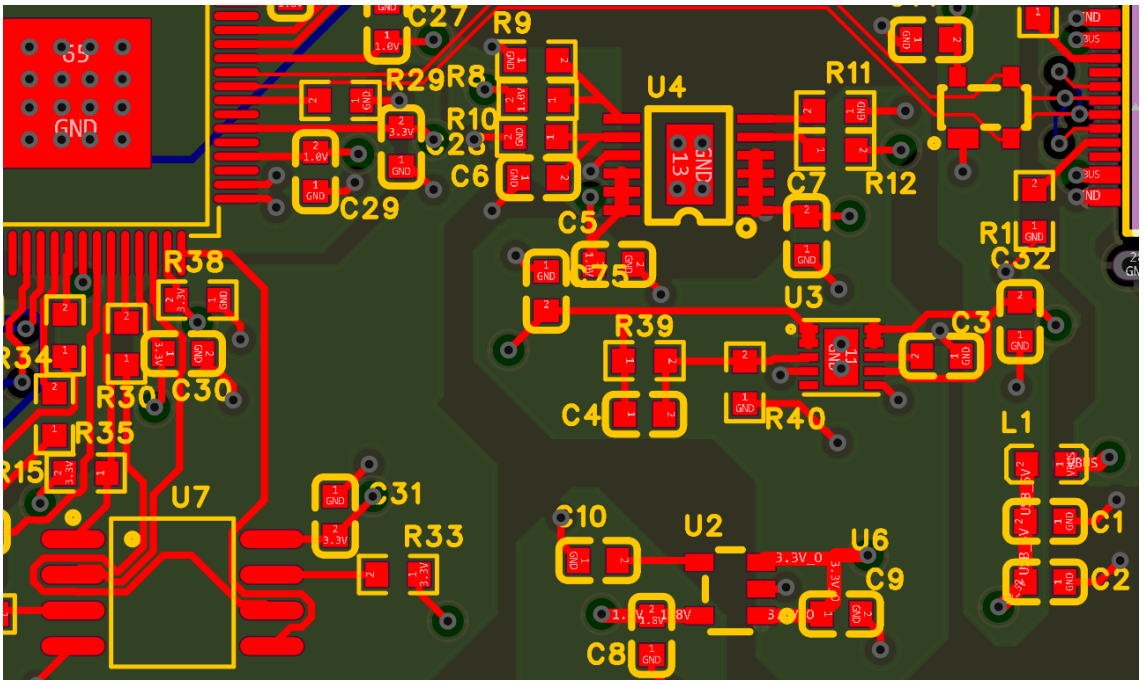


Figure 19: PDN region, U3 TPS7A9101, U2 SGM2036, U4 LT3045 1.0V, U6 TPD2E001, U1 USB-C

Figure 19 shows the complete power management and USB interface region. Reading from right to left — the physical direction of power flow — the USB-C connector U1 sits at the board edge with the BLM18PG ferrite bead L1 and bulk input capacitors C1 and C2 immediately downstream, forming the π-filter at the board's power entry point.

The TPS7A9101 (U3) sits centre-right with its feedback resistors R39 and R40 immediately adjacent, generating the 3.3V_O rail that feeds both the SGM2036 (U2) and the second LT3045 instance (U4). U2 and U4 are visible centre-left, their compact SOT-23-5 and MSOP-8 footprints occupying minimal board area. The TPD2E001DZDR (U6) sits between L1 and U1, intercepting ESD events on the USB data lines before they reach the MCU.

The 3.3V_O net routing is visible as a trace connecting U3's output to U2's VIN and U4's input — the physical implementation of the cascaded regulation architecture described in the PDN section.

3.5.6 XU208 MCU and Clock Region

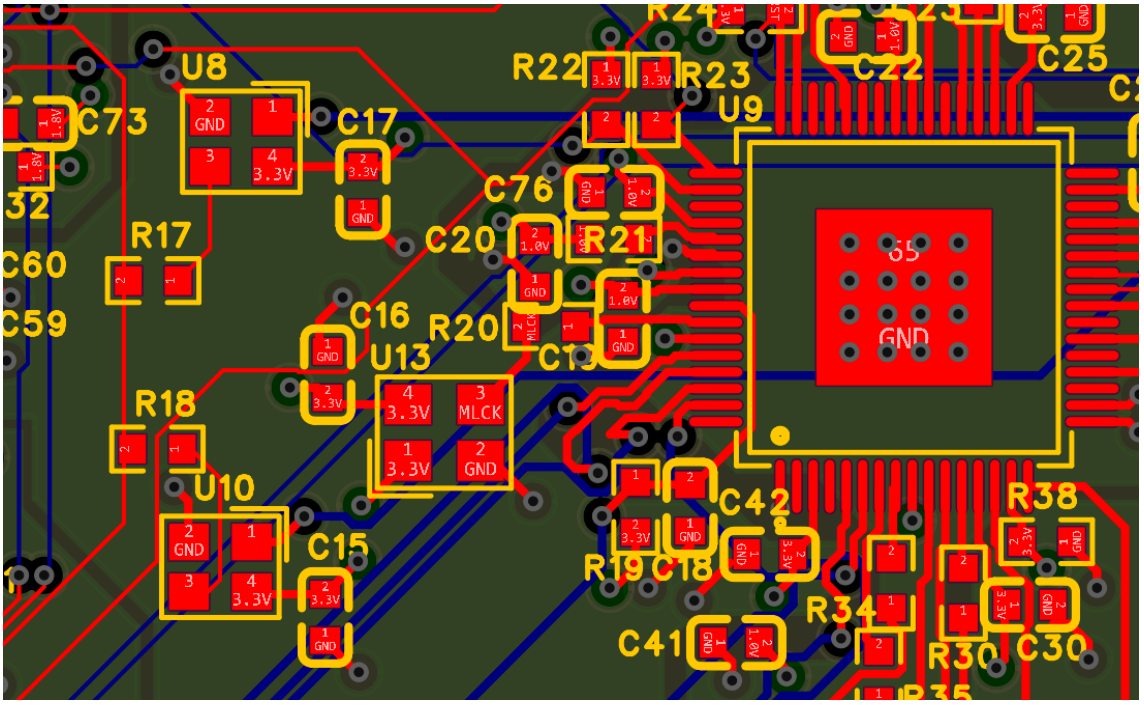


Figure 20:XU208 U9 central placement, clock oscillators U13 U10 U8, decoupling network

Figure 20 shows the XU208 (U9) at board centre — the large QFN package with its 4×4 exposed pad thermal via array clearly visible. The decoupling network surrounding the MCU is extensive: C20, C21, C29, C42, C76 and additional capacitors distributed around the perimeter provide localised supply stabilisation at each VDD pin of the package.

The three clock oscillators are visible left of the XU208: U13 (24MHz PLL reference) with its supply decoupling capacitor C16 immediately adjacent , U10 (22.576MHz, 44.1kHz family) below with C15, and U8 (24.576MHz, 48kHz family) above with C17. The MLCK trace routes from U13 directly into the XU208 clock input. R17 and R18 — the 22Ω series termination resistors on the audio master clock outputs — are placed immediately adjacent to U8 and U10's output pins respectively, implementing source termination at the driver end of each clock trace.

The physical proximity of all three oscillators to the XU208 minimizes clock trace length and therefore clock trace inductance, reducing pickup area for noise that

would modulate the clock signals and contribute to jitter at both the PLL and the DAC inputs.

3.5.7 Right CS43131 — U12 and Charge Pump Network

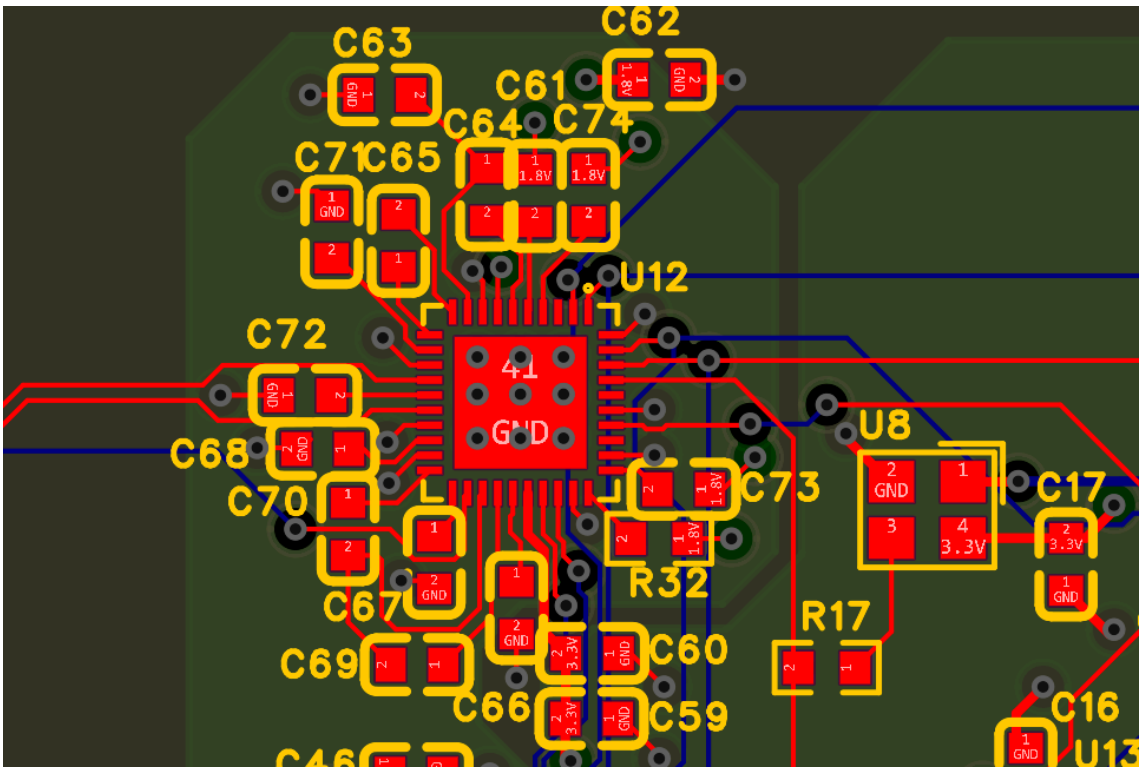


Figure 21: U12 right CS43131, charge pump network, U8 oscillator

Figure 21 shows the right channel CS43131 (U12) with its equivalent flying capacitor network. The symmetry with U11 is deliberate and physically visible — C61, C62, C63, C64, C65, C71, C72, C74 mirror the left channel placement as closely as routing constraints allow. The exposed pad via array (marked "41 GND") provides the identical thermal and electrical ground connection as U11.

U8 (24.576MHz) is visible lower-right with R17 inline on its MLCKD output trace — the clock routing from oscillator to CS43131 XTI/MCLK input maintaining consistent trace geometry throughout.

The blue traces visible routing through this region are Inner1 ground plane connections and Bottom Layer slow signals — the I2C configuration bus and

HP_DET_SIG detection routing that connect the CS43131 chips to the XU208 without crossing the high-speed top layer signal paths.

4. Failure Mode and Effects Analysis (FMEA) — Version 2 Second Revision

The following FMEA documents the identified failure modes of the Version 2, Second Revision design, their potential causes, effects on system operation, and the mitigation strategies implemented in the design. The analysis covers the five primary functional domains of the board: power distribution, USB interface, clock architecture, digital audio path, and analog output stage.

ID	Component/Domain	Failure Mode	Potential Cause	Effect on System	Severity (1-10)	Probability (1-10)	Detection (1-10)	RPN	Mitigation
F01	USB-C Connector U1	ESD transient on USB_DP/DN	Hot-plug event, static discharge	XU208 USB PHY damage, permanent enumeration failure	9	7	3	189	TPD2E001DZDR TVS diode clamps to safe level before MCU input; IEC 61000-4-2 Level 4 rated
F02	TPS7A9101 U3	Output voltage collapse	Input undervoltage, overcurrent, thermal shutdown	Loss of 3.3V_O rail; XU208 core and DAC supplies fail simultaneously	10	3	4	120	EN pin tied to USB_5V ensures clean enable; NR/SS soft-start prevents inrush collapse.

F03	LT3045 U4	1.0V core rail dropout	Excessive XU208 digital switching load, insufficient input headroom	XU208 core brownout; undefined firmware behavior, potential SPI flash corruption	9	3	5	135	200kΩ ILIM resistor sets current limit; 4.7µF output capacitor provides transient headroom; PGFB power-good monitoring
F04	SGM2036 U2	1.8V rail noise	Insufficient PSRR at switching frequencies of CS43131 charge pump	Elevated noise floor at DAC analog supply; degraded SNR and THD+N at output	7	4	6	168	Two-stage cascade: TPS7A9101 → SGM2036 provides double noise rejection; BP pin bandgap filtering
F05	W25Q32 U7	SPI boot failure	CS# line floating during power-up; spurious flash access corrupting firmware	XU208 fails to load sc_usb_audio firmware; no USB enumeration	9	3	4	108	R15 (10kΩ) pull-up on CS# ensures deselected state during power-up; dedicated 100nF decoupling on VCC
F06	XU208 U9	USB enumeration failure	PHY driver impedance mismatch	Device not recognised by host; complete loss of audio function	8	3	5	120	Impedance matched DP and DN lines, FR4 dielectric width
F07	XU208 U9	PLL lock failure	PLL_AVDD supply noise; 24MHz reference clock	I2S master clocks not generated; no audio output	8	3	6	144	R21 (4.7Ω) RC filter isolates PLL_AVDD from digital supply; dedicated C20/C76 decoupling; active

			instability						oscillator U13 provides low-impedance reference
F08	CS43131 U11/U12	I2C address conflict	Both ADR pins at same logic level	Both DACs respond to all I2C transactions; independent channel configuration impossible	8	2	7	112	U12 ADR pulled to 1.8V (address 1); U11 ADR pulled to GND (address 0); verified in schematic review
F09	CS43131 U11/U12	Charge pump instability	Incorrect flying capacitor values; 1.8V supply insufficient headroom	Output stage voltage collapse; distorted or absent headphone output	8	3	5	120	2.2µF flying capacitors per CS43131 application note; 15µF FILT+ reservoir capacitors; cascaded PDN ensures clean 1.8V supply
F10	NZ2520SH U8/U10	Master clock frequency error	Crystal oscillator tolerance; temperature variation	DAC sample rate mismatch; audio pitch error, increased jitter	6	2	7	84	NZ2520SH and NZ2520SDA temperature-compensated oscillators specified; 22Ω series termination on MLCKD outputs damps reflections
F11	PCB Assembly	Component tombstoning	0402 footprint reflow imbalance	Open circuit on passive components;	7	6	5	210	Migration to 0603 footprints in Second Revision specifically to reduce

				unpredictable circuit behavior					tombstoning risk during hand assembly
F12	PCB Assembly	Solder bridge on QFN pads	Fine-pitch QFN package hand soldering	Short circuit between adjacent supply pins; potential IC damage	8	5	4	160	Exposed pad via array provides visual inspection reference; stencil-applied paste recommended for QFN packages
F13	Ground Plane	Ground loop noise	Accidental ground plane cut during routing	Increased loop area; elevated EMI and noise floor	7	2	6	84	Unbroken Inner1 ground plane verified in EasyEDA DRC; no signal vias permitted to penetrate ground plane without clearance
F14	JTAG Header H1	Debug interface noise coupling	Long unshielded JTAG traces during active debugging	Noise injection into adjacent audio signal paths during firmware development	5	4	7	140	Multiple GND pins distributed throughout header minimize loop area; Bottom Layer routing separates JTAG from top-layer audio signals

Table 1

RPN = Severity × Probability × Detection. Higher RPN indicates higher risk priority. The highest RPN failure modes are F01 (ESD — 189), F11 (tombstoning — 210), and F12 (QFN solder bridge — 160). F11 and F12 are assembly-related rather than design-related, and both are mitigated by the 0603 footprint migration implemented in the Second Revision and careful hand-assembly practice. F01 is

mitigated at the design level by the TPD2E001DZDR. The remaining failure modes all carry implemented design mitigations and represent acceptable residual risk for a prototype assembly.

5. Discussion

5.1 Design Process Reflection

The development of this thesis followed an iterative engineering design cycle across two distinct architectures and three revisions, each transition driven by a concrete technical or economic constraint rather than an arbitrary design change. The progression from Version 1 to the final Version 2, Second Revision illustrates a fundamental principle of embedded hardware engineering: the gap between a technically ambitious specification and a deliverable design is rarely bridged by compromise on performance, but rather by architectural rethinking that achieves equivalent or superior outcomes through a different technical approach.

The Version 1 desktop architecture, while technically sophisticated in its simulation work — particularly the MOSFET-based capacitance multiplier achieving -112.12dB power rail SNR — was ultimately undeliverable within the project constraints. The financial burden of three toroidal transformers, the CNC-milled aluminum enclosure, and state-of-the-art components including the ESS9039Q2M DAC and ADAU1467 DSP, combined with the fundamental EMI incompatibility of integrating a WiFi and Bluetooth-enabled ESP32-C3 into a mixed-signal circuit, rendered the architecture infeasible. The decision to scrap Version 1 was not a failure of engineering — the simulation work demonstrated sound technical understanding — but a failure of initial scope definition. The lesson carried forward was the primacy of component availability and total system cost in the early design phase, before significant simulation work is invested in an undeliverable architecture.

The Version 2 CT7601CR architecture represented a well-reasoned pivot to a portable form factor, and the schematic work completed for this version was substantive. The fatal flaw — Comtrue's closed-source development environment with no available IDE or devkit — was not identifiable from the datasheet alone and only became apparent during the firmware bring-up planning phase. This represents a

component selection risk that is not captured by standard electrical specifications: the availability of a development ecosystem is as critical a selection criterion as any electrical parameter for an MCU. The XU208 replacement in the First Revision addressed this directly, and the open-source sc_usb_audio firmware stack and xTIMEcomposer Studio toolchain have a proven track record across the broader audio engineering community.

The Second Revision's primary contribution was engineering refinement rather than architectural change: the migration from 0402 to 0603 passive footprints, the complete re-verification of every passive component value against manufacturer application notes, and the finalisation of the cascaded PDN architecture. These changes reflect the reality of prototype hardware development — a schematic that is electrically correct can still produce an unassemblable board if manufacturing constraints are not considered from the outset.

5.2 Performance Analysis Against Design Objectives

The final design addresses each of the technical limitations identified in the State of the Art through specific architectural decisions whose justification is documented throughout this thesis.

The dual-mono CS43131-CNZR architecture provides complete physical channel separation at the DAC level, with the CS43131's specified interchannel isolation of greater than 110dB [9] applying to the full signal path rather than just the DAC core. This directly addresses the single-stereo DAC limitation common across the mid-range commercial segment, where interchannel crosstalk is limited by shared analog output stage components.

The three-oscillator clock architecture — 22.5792MHz and 24.576MHz crystal oscillators supplying the DAC chips directly, with a separate 24MHz reference for the XU208 PLL — eliminates the accumulated phase noise of PLL-derived clock multiplication from the audio signal path. The NZ2520SH and NZ2520SDA temperature-compensated oscillators [16] [17] provide stable frequency output across the operating temperature range, with the 22Ω source termination resistors on each MLCKD output damping transmission line reflections that would otherwise introduce periodic jitter at the DAC input.

The PDN architecture splits from USB_5V into two parallel first-stage regulators: U5 LT3045 serving the 3.3V digital logic rail directly, and U3 TPS7A9101 serving as the upstream conditioner for all noise-critical loads. From the TPS7A9101's 3.3V_O output, a second regulation stage cascades into U4 LT3045 (1.0V XU208 core) and U2 SGM2036 (1.8V DAC supply), providing two stages of noise rejection between raw USB_5V and the analog supply rails. The TPS7A9101's 4.4µV RMS output noise feeding into the downstream LT3045 and SGM2036 collectively ensures the 1.8V CS43131 supply rail is effectively isolated from the USB power bus noise that limits SNR performance in budget and mid-range devices with single-stage PDN architectures.

The 4-layer PCB with an unbroken Inner1 ground plane, high-speed signals on the Top Layer, power distribution on Inner2, and slow control signals on the Bottom Layer implements the electromagnetic compatibility principles of Henry Ott [21] directly in the physical design. The chamfered octagonal board outline and compact component placement demonstrate that the dual-mono architecture — which carries a component density penalty relative to single-stereo implementations — can be realised in a portable dongle form factor competitive with commercial products at the same price point.

5.3 Limitations and Outstanding Work

The primary limitation of this thesis at the time of submission is the absence of measured hardware results. The fabricated PCB is in transit at the time of writing, and the component assembly and testing phases documented in the intended verification methodology have not yet been completed. The performance claims made throughout this thesis are therefore based on simulation data, datasheet specifications, and established circuit theory rather than measured outcomes. The LTSPICE simulation of the Version 1 280V PSU demonstrated an 11.9V deviation from theoretical prediction due to non-ideal component behavior — a result that illustrates the gap between simulation and physical hardware that can only be resolved through measurement.

The firmware development phase using xTIMEcomposer Studio and the sc_usb_audio stack has not been completed. While the XMOS XU208 platform has a well-documented open-source firmware ecosystem and the hardware design follows the XU208 hardware design guide recommendations precisely, firmware bring-up on a

custom PCB invariably surfaces issues not visible in the schematic — timing violations, I2C address conflicts, SPI boot sequence errors — that require iterative debugging through the XTAG4 interface.

The FMEA identified component tombstoning during hand assembly (RPN 210) and QFN solder bridge formation (RPN 160) as the highest-risk failure modes. Both are assembly process risks rather than design risks and will be managed through careful hand-soldering practice and post-assembly continuity testing. The 0603 footprint migration specifically targets the tombstoning risk identified in the FMEA.

5.4 Comparison with Commercial Benchmarks

Against the commercial devices benchmarked in the Market Analysis, the final design occupies a technically competitive position. The dual-mono architecture, three-oscillator clock system, and cascaded PDN are features not found simultaneously in any bus-powered portable device at any price point in the current market. The XMOS XU208 platform is proven in desktop devices — the Topping D10 [6] and Khadas Tone 2 Pro [7] — but its adaptation to a bus-powered portable dongle within the USB 2.0 500mA current envelope represents a novel implementation not currently available commercially.

The component cost of approximately $60 positions the design competitively against the FiiO KA11 [3] at the same price point while offering a technically superior architecture — dual-mono vs single-stereo DAC, independent clocks vs PLL-derived, three-stage cascaded PDN vs single-stage. Against the iFi GO Bar [5] at $150, the design offers comparable architectural features at less than half the component cost, with the performance delta between the two dependent on measured hardware results not yet available.

6. Comparative Architecture Table

The following table documents the progression of design decisions across the four major versions of the project, illustrating the technical and economic constraints that drove each architectural transition.

Parameter	Version 1 (Desktop)	Version 2 (CT7601CR)	Version 2 Revision 1 (XU208 R1)	Version 2 Revision 2 (Final)
MCU	ESP32-C3	Comtrue CT7601CR	XMOS XU208-128-TQ64	XMOS XU208-128-TQ64-I 10
DAC	ESS9039Q2M	Cirrus Logic CS43131 (dual mono)	Cirrus Logic CS43131 (dual mono)	Cirrus Logic CS43131-CNZR (dual mono)
DSP	ADAU1467	None	None	None
Amplifier Topology	Vacuum tube + solid state op-amp	Integrated Class H	Integrated Class H	Integrated Class H
PSU Architecture	Triple transformer, quad full bridge + MOSFET capacitance multiplier	SGM2036 LDOs	LT3045 + SGM2036	USB_5V → LT3045 (3.3V digital logic); USB_5V → TPS7A9101 (3.3V_O) → LT3045 (1.0V XU208 core) + SGM2036 (1.8V DAC supply)
Clock Architecture	Single crystal + ESP32 PLL	Single 12Mhz crystal oscillator + PLL	Single 24MHz reference + PLL	Three independent oscillators (24MHz PLL ref, 22.5792MHz, 24.576MHz)
Output Stages	Planned 3.5mm SE + 4.4mm BAL	3.5mm SE + 4.4mm BAL	3.5mm SE + 4.4mm BAL	3.5mm SE + 4.4mm BAL

PCB Layers	4	4	4	4
Passive Footprint	Planned 0603/THT	0402	0402	0603
Ground Strategy	Planned Split planes (GNDA/GNDD/GND)	Planned Split planes (GNDA/GNDD/GND)	Split planes (GNDA/GNDD/GND)	Unbroken single ground plane
Firmware	ESP-IDF (open source)	Proprietary .bin (closed source)	Sc_usb_audio (open source)	sc_usb_audio (open source)
Development Environment	ESP-IDF / Arduino	Closed source — no IDE available	xTIMEcomposer Studio / XMOS Tools	xTIMEcomposer Studio / XMOS Tools
Form Factor	Desktop enclosure (CNC aluminum)	Portable board	Portable board	Portable board
Estimated Component Cost	>$500	~$40	~$80	~$60
Feasibility	Financially and technically infeasible in timeframe	Technically blocked by closed firmware	Functional architecture	Final submitted design
Fatal Flaw	Cost, EMI, transformer sourcing	No IDE, no open source firmware	0402 assembly risk, PDN incomplete	None identified — board in fabrication

Table 2

7. Commercial Benchmark Table

The following table benchmarks the final Version 2, Second Revision design against the commercial devices surveyed in the State of the Art, across the key technical parameters relevant to portable DAC/AMP performance.

Parameter	**JCally JM6 Pro**	**Jade Audio JA11**	**FiiO KA11**	**Moondrop Dawn Pro**	**iFi GO Bar**	**Topping D10**	**Khadas Tone 2 Pro**	**This Design (V2R2)**
MCU/ USB	Proprietary SoC	Proprietary SoC	Proprietary SoC	CT7601	XMOS	XMOS XU208	XMOS XU216	XMOS XU208

Processor								
DAC Architecture	Single chip integrated + AMP	Single chip integrated	Single stereo DAC	Dual DAC	Dual DAC	Single stereo DAC	Single stereo DAC	**True dual mono**
DAC Chip	Conexant CX31993 + MAX97220	Undisclosed	CS43131	CS43131	Burr-Brown	ES9038Q2M	ES9038Q2M	**CS43131-CNZR ×2**
Clock Source	PLL derived	PLL derived	PLL derived	PLL derived	Independent	Independent	Independent	**3× independent oscillators**
Output Topology	3.5mm SE only	3.5mm SE only	3.5mm SE only	3.5mm SE + 4.4mm BAL	3.5mm SE + 4.4mm BAL	RCA + 6.35mm	3.5mm SE + 4.4mm BAL	**3.5mm SE + 4.4mm BAL**
PDN Architecture	Single stage	Single stage	Single/dual stage	Unknown	Multi-stage	External PSU	External PSU	**Parallel first-stage (LT3045 3.3V + TPS7A9101 3.3V_O); TPS7A9101 cascades into LT3045 (1.0V) + SGM2036 (1.8V)**
Max Output (SE)	~60mW @32Ω	~30mW @32Ω	~200mW @32Ω	~120mW @32Ω	~300mW@32Ω	4.2VRMS	~125mW @32Ω	**Untested**
Balanced Output Power	None	None	None	~120mW @32Ω per chanel	~475mW@32Ω	None	~400mW @32Ω	**Untested**

Bus Powered	Yes	Yes	Yes	Yes	Yes	No	No	**Yes**
UAC2 Compliant	No	No	Partial	Yes	Yes	Yes	Yes	**Yes**
Max Resolution	32bit/384 kHz	32bit/384 kHz	32bit/384k Hz	32bit/384k Hz	32bit/384k Hz	32bit/384k Hz	32bit/768k Hz	**32bit/384k Hz**
Driverless macOS/Linux	No	No	No	Yes	Yes	Yes	Yes	**Yes**
Approximate Price	~$15	~$20	~$30	~$50	~$300	~$80	~$100	**~$60 component cost**

Table 3

8. Intended Testing and Verification Methodology

The following section documents the intended testing procedures to be conducted upon receipt of the fabricated PCB. Testing is structured in three phases: power-on verification, firmware bring-up, and audio performance verification.

8.1 Phase 1: Power-On Verification (Multimeter)

Prior to connecting any active components, continuity testing will verify the absence of solder bridges across all QFN exposed pads and fine-pitch component footprints using a digital multimeter in continuity mode. The following DC voltage measurements will then be taken at each regulated rail test point with the board powered from a USB-C source:

Test Point	**Expected Voltage**	**Acceptable Range**	**Instrument**

VBUS (post ferrite bead)	5.0V	4.75V — 5.25V	Multimeter
USB_5V (post L1)	5.0V	4.75V — 5.25V	Multimeter
3.3V rail (U5 output)	3.3V	3.2V — 3.4V	Multimeter
3.3V_O rail (U3 output)	3.3V	3.2V — 3.4V	Multimeter
1.0V rail (U4 output)	1.0V	0.95V — 1.05V	Multimeter
1.8V rail (U2 output)	1.8V	1.75V — 1.85V	Multimeter

Table 4

Any rail outside its acceptable range indicates a PDN fault — most likely an incorrect SET resistor value, a solder bridge on an LDO package, or an open circuit on a decoupling capacitor. The power-good indicators on the LT3045 instances provide additional diagnostic information: a logic-low PG output indicates the output voltage has not reached the 90% threshold set by the PGFB divider [10].

8.2 Phase 2: Firmware Bring-Up (XTAG4 + xTIMEcomposer Studio)

With PDN rails verified, the XMOS XTAG4 debug adapter will be connected to the FTSH-110-04-H-D JTAG header H1. The sc_usb_audio [26] firmware will be compiled in xTIMEcomposer Studio and flashed to the W25Q32JVSSIQ SPI flash via the XU208's JTAG interface. The following sequence will be performed:

First, the XU208 will be held in reset via the RST_N line on the JTAG header while the SPI flash is programmed. This prevents the XU208 from attempting to boot from an empty or partially programmed flash, which could produce undefined bus states on the SPI interface.

Second, following successful flash programming, RST_N will be released and the XU208 boot sequence will be monitored through xTIMEcomposer Studio's debug interface. Successful boot is confirmed by the appearance of the device as a UAC2 audio interface in the host operating system — on macOS this will appear in Audio MIDI Setup, on Linux via aplay(-1)

Third, the I2C configuration bus will be verified using the XU208's I2C master interface in xTIMEcomposer Studio — a successful register read from each CS43131 at its assigned address (U12 at address 1, U11 at address 0) confirms correct I2C addressing and DAC initialisation.

8.3 Phase 3: Audio Performance Verification (Oscilloscope + Multimeter)

With firmware operational and USB enumeration confirmed, audio performance verification will proceed using a digital oscilloscope and precision multimeter.

Supply Rail Noise Measurement: With the board streaming audio, the oscilloscope will be AC-coupled to each PDN rail to measure residual ripple and switching noise. The expected noise floor on the 1.8V DAC supply rail, given the two-stage cascaded regulation, should be below 1mV peak-to-peak. Any supply noise above this threshold indicates insufficient PDN attenuation and will be investigated through frequency domain analysis using the oscilloscope's FFT function to identify the noise source frequency.

Output Voltage Verification: A 1kHz 0dBFS sine wave will be played through the device at maximum volume. The RMS output voltage will be measured at both the 3.5mm and 4.4mm outputs using the multimeter's AC voltage function. Expected measurements are approximately 2VRMS at the 3.5mm output and 4VRMS differential at the 4.4mm balanced output, consistent with the CS43131 datasheet specification of 2VRMS per output pin.

Frequency Response: A swept sine wave from 20Hz to 20kHz will be applied at 0dBFS and the output voltage measured at each frequency point using the oscilloscope. The expected response is flat within ±0.5dB across the full audio band — any significant deviation indicates a coupling capacitor value error or a charge pump instability at specific frequencies.

Clock Verification: The oscilloscope will be used to verify the presence and frequency of the three clock signals — MLCK (24MHz at XU208 XTAL_IN), MLCKD from U8 (24.576MHz) and U10 (22.5792MHz) at the CS43131 XTI/MCLK inputs. Frequency accuracy will be verified against the oscilloscope's internal timebase. The 22Ω series termination resistors on each clock output will be verified for correct damping by observing the clock edge waveform — a well-terminated clock should show clean edges without ringing or overshoot exceeding 10% of the signal amplitude.

Headphone Detection: Inserting and removing a headphone plug into both the 3.5mm and 4.4mm outputs will verify the HP_DET_SIG detection circuit — successful detection is confirmed by the CS43131 asserting the INT line to the XU208, observable on the oscilloscope, and by the firmware responding with an impedance detection routine visible in the xTIMEcomposer debug output.

9. Conclusion

This thesis documents the complete design process of a portable USB-C DAC/AMP built on a 4-layer mixed-signal PCB, from initial concept through two distinct architectures and three design revisions to a fabricated board ready for assembly and testing. The design process demonstrated the iterative nature of hardware engineering: the Version 1 desktop architecture produced valuable simulation work — including a MOSFET-based capacitance multiplier achieving -112.12dB power rail SNR — before being replaced by a more deliverable architecture driven by financial and technical feasibility constraints. The Version 2 CT7601CR architecture was technically sound at the schematic level but fatally constrained by the closed-source firmware ecosystem of its MCU, leading to the replacement with the XMOS XU208 — a proven, open-source USB audio processor with an active developer community and a fully documented hardware design guide.

The final Version 2, Second Revision design implements a true dual-mono architecture using two independent CS43131-CNZR DAC/AMP chips, three independent crystal oscillators for jitter-free master clock distribution, a three-stage cascaded power distribution network isolating the analog supply chain from USB VBUS noise, and both 3.5mm single-ended and 4.4mm balanced outputs — all within a compact chamfered octagonal 4-layer PCB designed for bus-powered operation within the USB 2.0 500mA current envelope.

Component selection, circuit architecture, PCB stackup design, and electromagnetic compatibility decisions were derived directly from manufacturer application notes, hardware design guides, and established EMC literature — principally Henry Ott's Electromagnetic Compatibility Engineering [21] — rather than from supervised instruction. This independent approach produced a design whose technical architecture is competitive with commercial products at significantly higher price points and whose MCU platform adaptation — the XMOS XU208 in a bus-powered portable dongle — represents a novel implementation not currently available in the commercial market.

Upon receipt of the fabricated PCB, the intended verification methodology will validate the design through multimeter-based PDN rail measurement, XTAG4-assisted firmware bring-up and I2C bus verification, and oscilloscope-based audio performance measurement including supply rail noise, output voltage, frequency response, and clock signal integrity. The results of this testing phase will determine whether the simulated and theoretical performance predictions documented in this thesis are realised in the physical hardware.

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Appendix A: Bill of Materials

No.	Quantity	Comment	Designator	Footprint	Value	Manufacturer Part	Manufacturer
1	32	100nF	C1,C3,C15,C16,C17,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C40,C41,C42,C44,C55,C56,C57,C58,C60,C71,C72,C73,C74,C76	C0603	100nF	CT41G-0603-2X1-50V-0.1uF-K(N)	TORCH(火炬)
2	5	10uF	C2,C5,C11,C32,C75	C0603	10uF	GRT188D71A106ME13D	muRata(村田)
3	1	10nF	C4	C0603	10nF	GRT1885C1E103JA02D	muRata(村田)
4	6	4.7uF	C6,C7,C12,C13,C43,C59	C0603	4.7uF	GRM188B31C475KAAJD	muRata(村田)
5	4	1uF	C8,C9,C10,C14	C0603	1uF	GCM188D71H105KE36D	muRata(村田)
6	1	100nF	C18	C0603	100nF	GRM188B31H104KA92D	muRata(村田)
7	4	15uF	C45,C48,C61,C64	C0603	15uF	C1608X5R0J156MT000E	TDK
8	16	2.2uF	C46,C47,C49,C50,C51,C52,C53,C54,C62,C63,C65,C66,C67,C68,C69,C70	C0603	2.2uF	V225K0603X5R160NDT	VIIYONG(微容)
9	1	FTSH-110-04-H-D	H1	HDR-TH_FTSH-110-02-L-D		FTSH-110-04-H-D	SAMTEC
10	1	PJ-320D	J1	AUDIO-SMD_CIKI_PJ-320D_C2987375		PJ-320D	CIKI(皓富)
11	1	GT-3321667P-01	J2	AUDIO-TH_GT-3321667P-01		GT-3321667P-01	G-Switch(品赞)

12	1	BLM18PG331SZ1D	L1	L0603		BLM18PG331SZ1D	muRata(村田)
13	2	5.1kΩ	R1,R2	R0603	5.1kΩ	RMC06035.1K5%N	Tyohm(幸亚电阻)
14	2	402kΩ	R3,R8	R0603	402kΩ	RS-03K4023FT	FH(风华)
15	2	49.9kΩ	R4,R9	R0603	49.9kΩ	RMC060349.9K1%N	Tyohm(幸亚电阻)
16	1	33kΩ	R5	R0603	33kΩ	RMC1/16K333FTP	KAMAYA(釜屋電機)
17	2	249Ω	R6,R11	R0603	249Ω	PTFR0603B249RN9	RESI(开步睿思)
18	2	200kΩ	R7,R12	R0603	200kΩ	FRC0603J204 TS	FOJAN(富捷)
19	1	10kΩ	R10	R0603	10kΩ	HoAR0603-1/10W-10KR-0.1%-TCR25	Milliohm(毫欧)
20	1	10kΩ	R15	R0603	10kΩ	CRG0603J10K	TE Connectivity(泰科电子)
21	3	100kΩ	R16,R19,R33	R0603	100kΩ	SCR0603F100K	VO(翔胜)
22	7	22Ω	R17,R18,R20,R26,R27,R28,R30	R0603	22Ω	MMV03F22R0E	Ohmite
23	1	4.7Ω	R21	R0603	4.7Ω	TD03G4R70FT	FH(风华)
24	4	4.7kΩ	R22,R23,R24,R25	R0603	4.7kΩ	HoLTT0603-1/10W-4.7K-1%	Milliohm(毫欧)
25	1	43.2Ω	R29	R0603	43.2Ω	CR0603FA43R2G	LIZ(丽智电子)
26	2	0Ω	R31,R32	R0603	0Ω	RMC16JPTP	KAMAYA(釜屋電機)
27	2	33Ω	R34,R35	R0603	33Ω	SCR0603J33R	VO(翔胜)
28	1	3.3kΩ	R38	R0603	3.3kΩ	ARG03BTC3301	Viking(光颉)
29	1	3.57kΩ	R39	R0603	3.57kΩ	RS-03K3571FT	FH(风华)
30	1	1.15kΩ	R40	R0603	1.15kΩ	RTT031151FTP	RALEC(旺诠)

31	1	TYPE-C 16P CB1.6 073	U1	USB-C-SMD_SHOU_TYPE-C-16P-CB1.6		TYPE-C 16P CB1.6 073	SHOU HAN(首韩)
32	1	SGM2036-1.8YN 5G/TR	U2	SOT-23-5_L2.9-W1.6-P0.95-LS2.8-BR		SGM2036-1.8YN5G/TR	SGMICRO(圣邦微)
33	1	TPS7A9101DSKR	U3	SON-10_L2.5-W2.5-P0.50-TL-EP		TPS7A9101DSKR	TI(德州仪器)
34	2	LT3045IMSE#PBF	U4,U5	MSOP-12_L4.0-W3.0-P0.65-LS4.9-BL-EP		LT3045IMSE#PBF	ADI(亚德诺)
35	1	TPD2E001DZDR	U6	SOT-143_L2.9-W1.3-P1.92-LS2.3-BR		TPD2E001DZDR	TI(德州仪器)
36	1	W25Q32JVSSIQ	U7	SOIC-8_L5.3-W5.3-P1.27-LS8.0-BL		W25Q32JVSSIQ	Winbond(华邦)
37	1	NZ2520SH-24.57 6MHZ/NSA3579D	U8	OSC-SMD_4P-L2.5-W2.0-BL	24.576 MHz	NZ2520SH-24.576MHZ/NSA3579D	NDK
38	1	XU208-128-TQ64 -I10	U9	TQFP-64_L10.0-W10.0-P0.50-LS12.0-BL-EP5.3		XU208-128-TQ64-I10	XMOS
39	1	22.5792MHz	U10	OSC-SMD_4P-L2.5-W2.0-BL	22.5792MHz	NZ2520SB-22.5792MHZ-RNA3046A	NDK
40	2	CS43131-CNZR	U11,U12	TQFN-40_L5.0-W5.0-P0.40-TL-EP3.5		CS43131-CNZR	Cirrus Logic(凌云)
41	1	24MHz	U13	CRYSTAL-SMD_4P-L3.2-W2.5-BL	24MHz	XXHCCLNANF-24MHZ	TAITIEN(泰艺电子)